

Preface

More and more signal processing is being transferred to the digital domain to profit from the technological enhancement of digital circuits. Where technology scaling enhances the capabilities of digital circuits, it degrades the performance of analog circuits. However, it is important to note that the impact that technology scaling has on digital circuits is becoming smaller and smaller, which means that, in nanotechnologies, to enhance energy and area efficiency, we cannot simply depend on the benefits of this scaling. Although a share of the efficiency can be obtained from the technology, new circuit architectures and techniques have to be developed to really push the limits of efficiency.

In data converters, more specifically analog-to-digital converters (ADCs), a decision can be made: research energy and area efficient analog circuit techniques and architectures that cope with technological scaling issues, or design algorithms that use digital circuitry to assist the poor analog technological performance. The former option is the premise for the work developed in this book.

The work reported in this book explores various design techniques with the purpose of enhancing the power and area efficiency of building blocks mainly to be used in multiplying digital-to-analog converter-based ADCs. Therefore, novel analog techniques are developed for the three main blocks of an MDAC-based stage, namely, the flash quantizer, the amplifier, and the switched capacitor network of the MDAC. These techniques include self-biasing and inverter-based design for the flash quantizer and amplifier. Regarding the MDAC, it combines three techniques: unity feedback factor, insensitivity to capacitor mismatch, and current-mode reference shifting.

In the second part of this work, the designed amplifier is implemented and experimentally characterized demonstrating its practical feasibility and performance.

The final part of this work explores the design and implementation of a medium-low resolution high speed pipeline ADC incorporating all the developed circuits. Experimental results validate the feasibility of the techniques and demonstrate its attractiveness in terms of power dissipation and reduced area.