Preface

Sensors are ubiquitous in our lives and indispensable in many applications, e.g., process control, weighing scales, environmental monitoring, and temperature measurement. They can be found in wafer steppers, weighing scales, mobile phones and automobiles, etc. While these sensors convert the physical signals into electrical domain, their output voltage are small, in the millivolt-level, such as thermocouples and bridge transducers (thermistor bridges, Hall sensors and load cells). Therefore, they need amplifiers to boost such signals to levels compatible with the input ranges of typical Analog-to-Digital Converters (ADCs). To achieve sufficient signal-to-noise ratio, the input referred error of the amplifier should be reduced to a low enough level that means the amplifier must have low thermal and $1/f$ noise, high accuracy, and low drift. Achieving all these is quite challenging in today's mainstream CMOS technology whose inherent precision is limited by $1/f$ noise, component mismatch, gain error, and drift. A further challenge is to achieve good power efficiency since many sensor systems are battery-powered. This is also essential for precision temperature measurement to restrict local self-heating errors.

This book describes the use of power-efficient techniques to mitigate low frequency errors, resulting in interface electronics with high accuracy, low noise, and low drift. Since this book is mainly about techniques for eliminating low frequency errors, it describes the nature of these errors and the associated dynamic offset cancelation techniques used to mitigate them. It then shows how these techniques can be applied to operational amplifiers. Then these techniques are extended to current-feedback instrumentation amplifiers (CFIAs) which are well suited for bridge readout. Since the main disadvantage of CFIAs is their limited gain accuracy, the available techniques to improve this are discussed, such as resistor-degeneration, dynamic element matching, etc. The advantages and disadvantages of each of these techniques are analyzed.

Later, it presents the architecture design and implementation of a CFIA, in which a new technique (offset reduction loop) is proposed to suppress the chopper

ripple without causing noise folding. An improved version CFIA of the first CFIA is described, which maintains the noise performance of the first design and also achieves high gain accuracy without trimming. This is obtained by dynamic element matching and another proposed new technique (gain error reduction loop).

The basic architecture of the first CFIA is then combined with an ADC to build a readout IC. The system-level design of the readout IC together with implementation details and measurement results are presented. The CFIA and the ADC collaborate at system level to achieve an optimum performance. Measurement results show that the realized readout IC achieves state-of-the-art offset and drift performance.