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Advanced Gate Stacks for High-Mobility Semiconductors

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Preface

The continuous miniaturization of information processing and storage units has always been at the heart of advances in modern electronics. A large part of these advances is based on the evolution of bulk CMOS technology. Further progress is inhibited mainly by poor scaling of the transistor gate which causes short channel effects and results in overall performance loss. Part of the problem could be fixed by introducing SOI and/or multiple-gated devices (e.g., FinFETs, planar double gated, or tri-gated) which results in better electrostatic control of the channel. Further improvements could be made by using high mobility materials. In part, this has already been implemented since mobility enhancing strained Si is considered to be an irreplaceable part of next generation devices. By introducing high mobility semiconductors such as germanium (Ge) or III–V compounds it may be possible to enhance significantly the device performance for future generation nanoelectronics.

To develop a viable Ge MOS technology is a very challenging task. First, it is necessary to engineer compliant germanium-on-insulator (GeOI) substrates to ensure volume production at low cost. Second, it is important to develop appropriate surface passivation methodologies and high-k dielectrics in order to combine good electrical behavior with potential for gate scaling to equivalent oxide thickness less than 1 nm. Finally, it is necessary to master Ge processing to fabricate MOSFET devices with high $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio and enhanced channel mobilities. Since the first demonstration of functional Ge pMOSFETs with high-k dielectrics five years ago, there has been a lot of progress in bulk Ge transistors mainly using Si passivating layers and compressive strain which enhance p-channel mobility several times above Si/SiO_2 universal. On the other hand, there are also concerns that due to small energy gap, leakage current at source and drain as well as band-to-band tunneling will generate high OFF-state current especially in aggressively scaled Ge devices. Despite of this, with the right choice of device architecture (e.g., double-gated thin Ge films) and with the help of circuit design, power management and control should be possible so that junction leakage is not expected to be a serious obstacle. At the present time the biggest concern is that only Ge pMOSFETs perform

satisfactorily, while nMOSFETs either underperform or do not function at all for reasons which are not fully understood. The puzzling point is that all Ge surface passivating methods which benefit pMOSFETs have only minor influence on nMOSFETs so that channel mobility and ON-state currents in these devices remain low. This implies that there may be a fundamental materials problem which goes beyond surface passivation. Although this sets an interesting research scene in materials science and physics of devices it has also serious technological consequences. It implies that in future implementations of CMOS technology based on high mobility materials, the nMOS part should be made of materials other than Ge (e.g., strained Si or III–V compound semiconductors) co-integrated with Ge pMOS devices on the same complex engineered substrate.

The use of III–V channel materials for nMOS (instead of strained Si) is an attractive option due to their very high electron mobility. This means that III–V MOS technology must be developed and indeed not in competition to Ge but in compliance with it in a dual-channel CMOS approach. It is well-known that III–V transistor technology in the form of MESFETs and HEMTs exists since many years. However, this technology has been developed at the micron level and is appropriate for low density, low-noise analog circuits for niche market LSI applications. To transform this into a new III–V MOS technology which will follow the aggressive scaling rules of extremely dense mainstream circuits for ULSI digital applications is an extremely challenging task. Unlike the case of Ge, processing of III–V compounds in a standard or slightly modified semiconductor line using toolset and know-how similar to those applying for Si is very difficult. Issues related to self-aligned gate definition, implantation and high temperature activation annealing, etching and contact resistance must be addressed before we come any close to a viable MOS technology. In parallel, more fundamental materials and device architectural issues must be addressed. Channel materials (e.g., GaAs vs. InGaAs) and device structures (e.g., surface channels vs. buried channels) must be carefully selected for optimum performance. The device layer structure will also determine to some extent the operation mode (inversion, depletion or enhancement mode). Surface passivation of III–V compounds is a long-standing problem with no satisfactory solution yet. The main reason is the strong Fermi-level pinning at the oxide/semiconductor interface which is not fully characterized and quantified and, for that reason, not very well understood at the present time.

This book is a collection of review articles written by some of the key players in Ge and III–V research and development. The articles describe what could be considered as established knowledge after the renewal of interest in Ge and III–V MOS technology during the last five years of research. It is divided in four parts covering all areas from high mobility substrates, up to surface passivation and high-k gate preparation and characterization as well as field effect transistor fabrication and testing.

In chapters 1 through 3 the reader will find a review of mobility enhancing channels including strained Si and alternative orientations substrates.

Emphasis is given on (110)-oriented Si substrates with enhanced hole mobility making it particularly useful for pMOS devices. In addition, a review on the progress of GeOI substrates is given with a special emphasis on wafer bonding and layer splitting technique.

Chapters 4 through 7 describe Ge surface preparation, passivation, and gate dielectric emphasizing the characterization of interfaces between high-k dielectrics and semiconductors in an attempt to elucidate their role in the electrical behavior of the whole gate stack. Ab initio theoretical studies of oxide growth on semiconductors complement our knowledge about atomic configuration and binding principles at interfaces which determine band offsets.

In chapters 8 through 12 we present a number of analytical methodologies, including structural, chemical, physical, and electrical characterization of high-k oxides on Ge, GaAs, and Si. This is complemented by first principles calculations of dielectric properties (κ-values) and their correlation to the crystal symmetry and electronic structure. Point defects, band offsets interface reactions and interdiffusions are all related to the electrical behavior of gate stacks.

In chapters 13 through 17 we focus on the fabrication and characterization of field effect transistors made of Ge, III–V compounds and Si. Although basic transistor characteristics including channel mobility are studied using long-channel transistors, the scalability and manufacturability of Ge FETs is tested on the basis of short channel deep submicron transistors processed in a pilot Si line. In addition, the issues of Ge nanodevices are thoroughly discussed in connection with alternative architectures which will allow performance gain in future aggressively scaled devices based on Ge.

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