# Preface

Since Fairchild introduced the first commercially viable integrated circuit in Silicon Valley in 1957, the semiconductor industry has made impressive progress, particularly in communications, health, automotive, computing, consumer, security, and industrial electronics. This progress has followed Moore's Law, which predicts IC miniaturization down to nano dimensions and system-on-chip integration. At the same time, there are technologies based on or derived from silicon that do not scale according to Moore's Law such as RF, power electronics, sensors, MEMS, and lighting. These technologies are called "More than Moore."

Along with technology development trends characterized by Moore's Law and "More than Moore," business trends are characterized by cost reduction, shorter product life cycles, and outsourcing. The combination of these technology and business trends leads to increased design complexity, decreased design margins, increased probability of failures, decreased product development and qualification time, and challenges in assembly manufacturing. The quality and reliability of the assembly manufacturing process is critical in assuring a successful product. It is important to recognize that concurrent engineering of the semiconductor content and its high performance power package is becoming increasingly dependent on the rigorous use of proven multi-physics/FEA tools and techniques. The correct use of modeling tools can shorten power package design cycles but the challenge is insuring that the modeling tools and methodologies can support next generation products. Models for power packaging designs, materials, reliability and assembly manufacturing processes include electromigration simulation; diffusion along the interface of two metal materials; contamination at the interface between the lead frame, multiple chips, and epoxy mold compound (EMC); thermal resistance definition in multiple die power system in package (SiP) or the power module; 3D copper stud bumping and wire bonding simulation.

In the semiconductor industry, we all understand the importance of design, material selection, assembly manufacturing, reliability, and testing in minimizing power packaging failures. Wire bonding and stud bumping processes can induce silicon cratering, bond pad peel off, and cracking of the interlayer dielectric (ILD)

under the bond pad. Thin power die (below 50 μm) can crack when picked up from the tape. Molding can induce failures such as delamination due to voids in the interface between the lead frame and EMC. Lead frame forming, punch/singulation and trim may result in die and package cracking due to the impact. Tiny defects induced in an initial assembly process can impact quality in later assembly processes becoming a potential product quality and reliability concern. For example, during wafer sorting, cratering/marks can be induced on the bond pad. Later during wire bonding, when the wire is bonded to the cratered/marked bond pad, the adhesion strength at the interface between the wire bond and the bond pad can be compromised.

Power electronics packaging is rapidly advancing due to the increased market demand in almost all areas of power applications such as portable, consumer, home, computing, and automotive electronics. Due to its intrinsic structural nature, the performance requirements for power products are extremely high, especially due to their thermal and electrical environments. The materials and structural layout of power electronics makes the design rules and development of power packaging quite different from the development of regular IC packaging. The development of power packages depends heavily on power device integration. Current power devices have two major integration modes: Monolithic integration and hybrid integration. Monolithic integration includes power integrated circuits, high voltage integrated circuits (HVIC), and intelligent discrete power devices, combined with functional integration and the integration of passive elements. Hybrid integration includes the standard power module and the intelligent power module (IPM). This book presents a state-of-the-art and in-depth overview of power electronic packaging design, assembly processes, material characterization, reliability, and modeling. Recent advances in power electronic packaging are presented based on the development of power device integration. The book also covers how advances in both semiconductor content and advanced power package design and materials have co-enabled significant advances in power device capability during recent years. Extrapolating the same trends in representative areas for the remainder of the decade serves to highlight where further improvement in materials and techniques can drive continued enhancements in thermal management, usability, efficiency, reliability, and overall cost of power semiconductor solutions.

This book is arranged into 12 chapters. The first chapter introduces the challenges of power electronics packaging development, which include the impact of die shrinkage; power system on chip (SoC) vs. system in packaging (SiP); power package foot print pitch; and new power packaging materials. Chapter 2 describes electrical isolation design for power packaging, including design rules for isolation, estimation of clearance and creepage distances, power package design layout considerations, and application categories and standards. Chapter 3 discusses discrete power MOSFET package design and analysis. This chapter covers the trends for epoxy molding compound use; trends for current carrying capability; low Rds(on) and multiple direction heat transfer; typical discrete power package design and constructions; power VDMOSFET wafer level chip scale package (WLCSP) with Cu stud bumping; and trends of discrete power WLCSP. Chapter 4 regards

power IC packaging design, which includes power IC technology evolution; trends of high power density at the die level; smaller package foot prints and typical package design and analysis. Chapter 5 addresses the development of power module/SiP/Stack/3D/Embedded die package design and considerations, including the side by side die placement power system in packaging and module for low and high power applications; power stack die SiP; wafer level power stack die packaging with through silicon via (TSV); stack/embedded power module and integrating the power package with active and passive chips. Chapter 6 reviews thermal management, design, analysis and cooling for power packaging, including thermal resistance and measurement methods; selection of thermal test boards; thermal prediction, management and design including from device to board and multiple die thermal analysis; cooling design for power packaging. Chapter 7 discusses the material characterization for power packaging including the polyimide coating behavior on MOSFET die; die attach delamination characterization; EMC characterization; the mechanical and thermal behavior of ceramic and direct bond copper (DBC) substrates; solder material characterization; lead frame material testing and MOSFET material behavior in copper wire bonding. Chapter 8 presents typical assembly processes for power packaging, which include wafer handling; die pick up; die attach; wire bonding; molding; and trim/singulation. Chapter 9 introduces typical power packaging reliability testing which includes thermal and power cycling; passivation crack analysis; wafer probing; drop test and moisture related reliability analysis. Chapter 10 discusses power packaging modeling including the role of modeling; challenges of modeling tools; modeling requirements; modeling methodologies and modeling trends. Chapter 11 introduces codesign automation simulation for power packaging that includes thermal modeling and test correlation; wafer level power package parameter thermal simulation and thermal–mechanical, hygroscopic and vapor pressure codesign automation. Lastly, Chapter 12 presents power package electrical and multiple physics simulation. It consists of four sections: electrical simulation for resistance, inductance and capacitance (RLC); current capability; power unclamped inductive load (UIL) test or unclamped inductive switching (UIS) test and simulation, and electromigration simulation. Each chapter has a summary for the related design and methodology. The author hopes this book provides good reference material for researchers, design engineers, managers, university professors, and students who work on power electronics.

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