Chapter 2
Additive Processes for Semiconductors and Dielectric Materials

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Abstract This chapter presents an overview of the key methods and process recipes commonly employed in the deposition of semiconductor and dielectric thin films used in the fabrication of microelectromechanical systems (MEMS). These methods include chemical vapor deposition, epitaxy, physical vapor deposition, atomic layer deposition, and spin-on techniques. The materials featured in this chapter include silicon and its oxide, nitride, and carbide derivatives, silicon–germanium, diamond and diamondlike carbon, III-V semiconductors, aluminum oxide, and other notable semiconductor and dielectric materials used as structural, sacrificial, and passivation layers. The process recipes presented in this chapter largely come from publications that report not only processing details, but also key material properties of importance to MEMS that result from the reported processes. Whenever possible, the references included in this chapter are papers that are readily available via commonly used electronic databases such as IEEE Xplore™ and ScienceDirect™ so as to aid the reader in gathering more detailed information than can be practically presented herein. Furthermore, the processes selected for inclusion in this chapter were, for the most part, successfully used in the fabrication of MEMS structures or components, thus verifying their utility in MEMS technology. For select materials, case studies are included to provide process-related details that cannot easily be tabulated but are nonetheless of critical importance to successful usage of the process.

2.1 Overview

Semiconductors and dielectrics constitute the two most heavily utilized material classes in the MEMS fabrication toolset owing in large measure to the key properties of these materials. The rapid development of MEMS technology during the late

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R. Ghodssi, P. Lin (eds.), *MEMS Materials and Processes Handbook*,
MEMS Reference Shelf, DOI 10.1007/978-0-387-47318-5_2,

1980s and throughout the 1990s can be attributed to the ability to leverage heavily the expertise, know-how, and physical infrastructure developed for silicon and its oxide and nitride derivatives for the silicon IC industry. And although MEMS continues to benefit from advancements in processing technologies made for the silicon IC industry, MEMS also benefits from the emergence of new semiconductors and dielectric materials that are being developed for application areas that are not compatible with silicon as the principle material.

This chapter focuses on additive processes for semiconductor and dielectric materials for MEMS. These materials include those commonly used in the IC industry such as polysilicon, silicon dioxide, silicon nitride, and silicon–germanium, as well as other semiconductors, such as gallium arsenide, indium phosphide, and silicon carbide. Newly emerging semiconductors such as diamond and gallium nitride are also included, as well as dielectrics such as aluminum oxide. Like most thin films, some of the key properties of these materials are linked to the methods and specific recipes used to create the thin films. The principle purposes of this chapter are threefold: (1) to provide an overview of the common semiconductors and dielectrics used in MEMS technology, (2) to examine the methods used to deposit thin films of these materials, and (3) to provide an in-depth review of actual process recipes used to deposit the films and the key MEMS-centric material properties that result from proper execution of these recipes.

The chapter is organized by deposition technique and for each technique, by material. Each section is constructed around a set of data tables that contain key processing parameters along with associated material properties. The chapter is constructed in this manner to give the reader the ability to quickly perform side-by-side comparisons between recipes and resulting properties. As stated previously, the references used in this chapter are widely available in common electronic databases so that the reader can further investigate promising recipes by referring directly to the published work. This approach enables inclusion of a much larger body of information than can be accommodated with the summary-based approaches used in most reviews. For quick reference, Table 2.1 lists the materials and the deposition techniques described in detail in this chapter.

2.2 Thermal Conversion

This section presents an overview of the most common thermal conversion process used in the fabrication of MEMS devices: thermal oxidation of silicon, and describes general aspects of thermal oxidation of silicon, specific methods used in thermal oxidation, specific oxidation recipes, important material properties that result from these recipes, and some unconventional, MEMS-centric applications of thermal oxidation.

2.2.1 Process Overview

Silicon's position as the dominant semiconductor in modern IC technology can, in large part, be attributed to the passivating oxide that can be readily formed on its

Table 2.1 Additive processes used to deposit semiconductor and dielectric films used in MEMS fabrication as detailed in this chapter

Material	Thermal conversion	LPCVD	APCVD	PECVD	Epitaxy	PVD	ALD/ ALE	Spin cast
Silicon		X		X	X	X		
Silicon dioxide	X	X		X		X		X
Silicon nitride		X		X				
Silicon–germanium		X		X				
Germanium		X						
Silicon carbide		X	X	X	X	X	X	
Diamond		X						
Carbon/DLC[a]				X		X		
Gallium arsenide					X			
Indium phosphide					X			
Ternary III-V					X			
Gallium nitride					X			
Aluminum oxide							X	
Zinc oxide							X	

[a]DLC = Diamondlike carbon

surface. Commonly referred to by process engineers as "silicon oxide" this material is technically "silicon dioxide" in chemical composition. Silicon dioxide (SiO_2) naturally forms on the surface of Si by a process known as oxidation. Oxidation is a thermally driven conversion process that occurs over a very wide range of temperatures, including ambient conditions. If grown at room temperature, the material is known as a "native oxide" and has a thickness of roughly 1–2 nm. For MEMS applications, much thicker oxides (hundreds of nm to several microns) are typically required, necessitating the need for processing tools to produce such films. Of all the thin-film growth processes used in MEMS, oxidation of silicon is one of the most straightforward owing to the simplicity of the process. Known as thermal oxidation, the key ingredients aside from the silicon substrate itself are elevated temperature and a gaseous oxidant. Although a thin oxide can be formed on silicon under ambient conditions, oxides with thicknesses of relevance to MEMS (i.e., > several hundred nm) require temperatures of around 1000°C to be grown in a reasonable amount of time. Thermal oxidation is primarily performed at atmospheric pressure in an oxidizing environment that can be comprised of O_2, a mix of O_2 and H_2, or water vapor. Oxidation in O_2 is referred to as "dry oxidation" whereas oxidation in water vapor or mixtures of O_2 and H_2 is known as "wet oxidation."

Without question, thermal oxidation of silicon is the most thoroughly studied and well understood of all the film growth processes used in MEMS due to its critical importance in IC processing. From an engineering perspective, the most common and useful model to describe the oxidation process is known as the Deal–Grove model for thermal oxidation. This model describes the process in terms of several

fluxes, namely: (1) flux of oxidants from the main gas flow regime of the oxidation furnace to the substrate surface, (2) flux of oxidants through a pre-existing oxide to the oxide/Si interface, and (3) flux that describes the chemical conversion process. Oxidation reactors, commonly called furnaces, are operated in steady-state mode, meaning that key processing parameters such as temperature and oxidant flow rates are held constant with respect to time once the process is initiated. Steady-state considerations require that the three fluxes be equal, therefore the lowest flux will ultimately determine the oxidation rate. Reactors are constructed and operated in such a way that the flux of oxidants through the gaseous environment is not the rate-limiting flux, allowing the oxidation rate to be determined by the remaining two fluxes. The flux of oxidants through the pre-existing oxide is governed by the diffusion properties of the oxidant in SiO_2 whereas the flux at the oxide/Si interface is governed by reaction kinetics. Both fluxes are temperature dependent, increase with increasing temperature, and depend on the properties of the oxidant. The Deal–Grove model handles both the diffusion characteristics and kinematic properties of the process by assuming that the relevant first-order information for a particular oxidation process can be adequately quantified in terms of proportionality constants. As such, the diffusion properties of an oxidant in SiO_2 are described by its diffusivity, and information about the interfacial reactions of the oxidant with Si is represented by a constant known as the interface reaction rate constant. Equations (2.1) and (2.2) represent mathematical expressions for the fluxes associated with oxidant diffusion through the oxide and the interfacial reactions, respectively.

$$F_{\text{diffusion}} = D(C_0 - C_{\text{I}})/x_0 \tag{2.1}$$

$$F_{\text{reaction}} = k_{\text{i}} C_E \tag{2.2}$$

where C_0 is the oxidant concentration at the surface, C_{I} is the oxidant concentration at the SiO_2/Si interface, D is the diffusivity of oxidant in SiO_2, x_0 is the thickness of the resulting oxide and k_{i} is the interface reaction rate constant.

From a processing perspective, Equations (2.1) and (2.2) are not very useful in determining the final oxide thickness because it is difficult to quantify the oxidant concentrations at the SiO_2 surface and at the oxide/Si interface. However, further mathematical analysis yields an expression for the final oxide thickness that utilizes input parameters that have been determined from empirically derived data. Equation (2.3), known as the linear parabolic growth law, expresses oxide thickness in terms of oxidation time.

$$x_0^2/B + x_0/(B/A) = t + \tau \tag{2.3}$$

where t is the oxidation time and τ is given by the following expression,

$$\tau = (x_{\text{i}}^2 + Ax_i)/B \tag{2.4}$$

where x_{i} is the initial oxide thickness and x_0 is the final oxide thickness.

In Equation (2.3), B is known as the parabolic rate constant and is proportional to the diffusivity constant, whereas B/A is known as the linear rate constant and is proportional to the interface reaction rate constant. For thermal oxidation of Si, both the linear and parabolic rate constants B/A and B have been determined from empirical data and are readily available to the process engineer. As expected, these parameters exhibit a strong temperature dependence as shown in Equations (2.5) and (2.6) below.

$$B = C_1 \exp(-E_1/kT) \tag{2.5}$$

$$B/A = C_2 \exp(-E_2/kT) \tag{2.6}$$

where C_1 and C_2 are constants and E_1 and E_2 are activation energies. In these expressions, the constants and activation energies are readily available, enabling simple calculation of the linear and parabolic rate constants, and therefore a straightforward calculation of either oxidation time or oxide thickness.

As mentioned previously, the parabolic rate constant is proportional to diffusivity and the linear rate constant is proportional to the interfacial reaction rate constant. Consequently, the parabolic rate constant will depend on the oxidant and the linear rate constant will depend both on the oxidant and the crystalline orientation of the Si substrate. As such, the parameters needed to calculate these constants using Equations (2.5) and (2.6) have been determined for each oxidation process (dry, wet, and steam) as well as crystal orientation. In the case of the linear rate constant (B/A), it has been found that the relationship between this constant and the three technically relevant crystal orientations of Si is as follows:

$$(B/A)_{111} = 1.68(B/A)_{100} \tag{2.7}$$

$$(B/A)_{110} = 1.45(B/A)_{100} \tag{2.8}$$

A detailed description of the oxidation process, including a thorough development of the Deal–Grove model, as well as the data required to calculate oxidation times and thicknesses can be found in nearly any advanced undergraduate or graduate text on silicon VLSI fabrication technology, including two notable texts commonly used by MEMS process engineers [1–3].

Figure 2.1 is a schematic diagram of a standard oxidation furnace. The furnace consists of a long cylindrical fused quartz tube sized in length and diameter to hold large numbers (sometimes > 100), large diameter (i.e., 200 mm) Si wafers. Thermal oxidation is a conversion process using a gaseous source as the oxidant, so wafers can be loaded in a close packed configuration, with separation distances of a few millimeters being very common. The quartz tube is jacketed by a resistive heater that can reach temperatures in excess of 1200°C. The process is performed at atmospheric pressure and therefore vacuum sealing is not required. When not in use, the furnace is idled at a low temperature (600–800°C) and continuously flushed with an inert gas such as nitrogen. During operation, the inert gas is displaced by the oxidant, thus no vacuum pumping system is used. A gas manifold equipped with mass

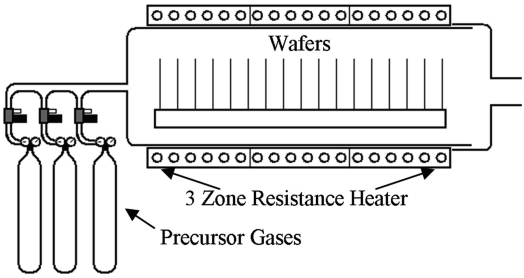

Fig. 2.1 Schematic diagram of a typical oxidation furnace

flow controllers is used to supply the furnace with the proper flow rates and relative concentrations of oxidant gas species.

The typical thermal oxidation process begins with a thorough cleaning of the Si wafers. The standard cleaning process is known as the RCA clean. The main purpose of the RCA clean is to ensure that any organic, ionic, and metallic contaminants are removed from the wafers prior to high-temperature processing. The process, detailed in Table 2.2, consists of a series of aqueous chemical baths into which the wafers are immersed for a prescribed length of time. Each bath is designated to remove a particular class of contaminants, and all aqueous processing, including rinses, is performed in deionized water. At the conclusion of the process, the wafer surfaces meet the cleanliness standards of CMOS processing. Although MEMS structures are generally not as sensitive as MOS transistors to such contamination, performing an RCA clean prior to each oxidation ensures that cross-contamination is kept to an absolute minimum.

Table 2.2 The RCA cleaning process[a]

Process step	Purpose	Details
RCA-1	Removed organics and metals	500 ml NH_4OH (29%) 500 ml H_2O_2 (30%) 2.7 l DI water 15 min at 70°C
HF Dip	Removes oxide formed during RCA-1	5 l DI water 100 ml HF (49%) 30 s
RCA-2	Removes alkali ions and cations	500 ml HCl (32–38%) 500 ml H_2O_2 (30%) 2.7 l DI water 15 min at 70°C

[a]Used in the Microfabrication Laboratory at Case Western Reserve University. The process is designed for a single batch of 25, 100 mm-diameter wafers.
1. Each step of the process is followed by a rinse in deionized water
2. After the final rinse, the wafers are spin–rinse dried
3. If necessary, a piranha clean is performed prior to RCA-1 in order to remove excessive organic and/or metallic contaminants

Once the wafers have been cleaned, they are ready for loading into the oxidation furnace. Once loaded, the furnace temperature is ramped up from its idle setpoint to the designated oxidation temperature, and the inert purge gas is displaced by the gaseous oxidant. The oxidation process proceeds under steady-state conditions until the desired oxide film is grown, after which the oxidant is displaced by the inert purge gas and the furnace temperature is ramped to its idle state.

2.2.2 Material Properties and Process Selection Guide for Thermal Oxidation of Silicon

Because the thermal conversion process occurs at the buried oxide/Si interface, thermal oxidation is inherently a diffusion-driven, self-limiting process. As a result, the maximum practical oxide thickness that can be obtained is about 2 μm. At this thickness, thermal oxides can be used for a wide range of applications, including masks for selective-area doping, etch masks for silicon bulk micromachining, and sacrificial layers for polysilicon and silicon carbide surface micromachining. Unlike other materials commonly used in MEMS, thermal SiO_2 films can only be grown on silicon substrates, thereby limiting their applicability in multilayered structures. That being said, thermal oxidation is not restricted to single crystalline Si wafers, but can also be performed to produce SiO_2 on polysilicon films, for as long as the materials beneath the polysilicon layer can tolerate the high temperatures associated with the oxidation process. Thermal oxides can also be grown on silicon carbide substrates, albeit at a much lower rate than for silicon [4].

At a given temperature, wet and steam oxidation rates are higher than dry oxidation rates, an effect that has been attributed to higher oxidant solubilities (i.e., H_2O) in SiO_2 than O_2. As such, thick oxides, such as would be required for masks used in dopant diffusion or solution-based bulk micromachining, are generally grown using wet or steam oxidation processes. Dry oxidation, on the other hand, is typically used to form the gate oxide in MOS transistors owing to its better electrical properties, but can be used in any application that does not require thick oxides (>500 nm).

Table 2.3 details the key thermal oxidation processes performed in the Microfabrication Laboratory at CWRU and is provided here to give the reader a sense of how process parameters such as gas flow relate to furnace size. As with many other MEMS fabrication facilities, oxidation is performed in commercially available, high-thoroughput systems. Due at least in part to the simplicity of the oxidation process, most commercial systems operate in much the same manner, and any significant process differences are likely due to scaling issues associated with differences in reactor geometry. For reference purposes, the system at CWRU is an MRL Industries™ Model 1118 which accommodates a 1.93 m long, 235 mm diameter quartz tube.

Thermal oxides have many properties that are attractive to silicon-based ICs and MEMS [1]. Thermal SiO_2 has a resistivity between 10^{14} and 10^{15} Ω cm, a dielectric strength of 5×10^6 V/cm and a dielectric constant of 3.9, making it exceptionally

Table 2.3 Thermal oxidation processes performed in the MRL industries™ model 1118 system at CWRU[a]

Type	Temp (°C)	Source gases	Flow rates	Growth time	Thickness (nm)
Dry oxidation	1050	O_2	6 slm	30 min	20
				1 h, 30 min	130
				3 h, 40 min	200
Wet oxidation	1075	O_2	6 slm	25 min	300
		H_2	10 slm	1 h, 35 min	500
				3 h, 55 min	1000
				10 h	2000

[a]The furnace idle temperature is 800°C. Typical ramp up and ramp down times are 60 and 90 min, respectively

well suited for electrical isolation, especially for electrostatically actuated devices. Silicon dioxide has an extremely high melting point (1700°C) and a low thermal conductivity (0.014 W/cm °C), especially when compared with Si. The etch rate in buffered HF (commonly used when photoresists are used as etch masks) is nominally 100 nm/min. As with every electrical insulator, SiO_2 has a large electronic bandgap at 9 eV and low electron mobilities (20–40 cm^2/Vs). The mass density of thermal oxide is 2.27 g/cm^3.

Thermal oxide has a thermal expansion coefficient of $5 \times 10^{-10}/°C$, which when compared to Si leads to a significant buildup of residual stress when oxidized silicon substrates are cooled to room temperature. Table 2.4 summarizes published data regarding the mechanical properties in wet thermal oxides. In both cases, the stress is moderately compressive. This level of stress would be more than sufficient to induce measurable bow in the Si wafer substrates; however, the typical oxide furnace configuration enables simultaneous oxide growth on both sides of each wafer, thereby negating the effect, especially when double-side polished wafers are used. In many MEMS applications, stress in thermal oxides is of secondary concern because the films are used as sacrificial layers or are patterned into small isolated structures.

Table 2.4 Residual stress in thermal SiO_2 films

References	Temp (°C)	Source gases	Thickness (μm)	Residual stress (MPa)	Plain strain modulus (GPa)	Fracture stress (GPa)
[5]	1000	O_2/H_2	433	–331		
[6]	950–1050	O_2/H_2	0.5–1	–258	49	0.89

2.2.3 Case Studies

By virtue of the fundamental nature of the thermal conversion process, there is very little process-dependent variation in the physical properties of thermal oxide films. Likewise a high degree of standardization in the industry has led most fabrication facilities to use very similar processes. As such, interesting case studies involving thermal oxide films don't involve links between specific process parameters and measured film properties, but rather creative ways to utilize thermal oxides as sacrificial layers to create Si structures that would otherwise be difficult to fabricate using conventional etching techniques. For example, Desai et al. described a process to fabricate silicon nanoporous membranes using a thermal oxide as a sacrificial material for pore formation [7]. The process involves the growth of a thin (20–100 nm) thermal oxide on a boron-doped Si substrate that is photolithographically patterned and etched to form an array of vias. The oxide grows uniformly on all exposed Si surfaces, including the vertical sidewalls of the vias. A boron-doped polysilicon film is then deposited onto the oxidized substrate, completely filling the vias and encasing the thermal oxide. The polysilicon is patterned to allow access to the thin oxide on the sidewalls of the vias. A freestanding single crystalline/polycrystalline membrane is then fabricated by selectively removing the Si substrate from the backside up to the boron-doped region. Nanopores are then fabricated in the membrane by etching the thin, vertically oriented thermal oxide in HF. Use of thermal SiO_2, the ability to grow a uniform oxide on vertically oriented Si surfaces by thermal oxidation, and the ability to control the oxide thickness by proper selection of temperature and oxidation time enables the fabrication of highly uniform (± 1 nm) nanopores using conventional microscale fabrication techniques.

2.3 Chemical Vapor Deposition

Section 2.3 reviews the use of chemical vapor deposition as an additive process for semiconductors and dielectrics in MEMS. This section begins with an overview of a generic chemical vapor deposition process and is followed by a detailed description of specific CVD methods commonly used in MEMS fabrication. This section continues by describing specific semiconductor and dielectric materials deposited by CVD, including specific deposition recipes and important material properties that result from these recipes. Where appropriate, case studies that illustrate key aspects of the CVD films are included.

2.3.1 Process Overviews

2.3.1.1 Introduction

Chemical vapor deposition (CVD) is the most widely employed means to deposit semiconductor and dielectric materials used in MEMS. In a general sense, CVD

is a process where a thin film is formed by the deposition of vapor-phase components onto a heated substrate. The vapor is comprised of gases that contain the constituents of the thin film. These source or precursor gases are introduced into the CVD reactor in a regulated manner so as to control the gas mixture and deposition pressure. Process parameters such as gas flow, reactor pressure, and substrate temperature are highly regulated so that the precursors dissociate into the proper reactive components such that the desired material is formed on the substrate surface and not in the vapor, because vapor-phase reactions could lead to unwanted particulate contamination of the substrate surface and pinholing in the films.

CVD has several key characteristics that make it the dominant deposition method for semiconductors and dielectrics in MEMS. For silicon and its derivatives, high-quality precursors that will readily dissociate into reactants at reasonable temperatures are commercially available. In most cases, the precursors are in the gas phase at room temperature, making delivery to the reactor and flow control relatively simple. In some cases, the precursors are in the liquid phase at room temperature. In these instances, an inert gas such as nitrogen, or a reactive gas such as hydrogen, can be used as a carrier gas to deliver precursor vapor to the reaction chamber. In many cases, the gaseous precursors are diluted in a carrier gas at the source to enable safe storage. Along similar lines, precursor gases for conductivity modification, commonly known as doping gases, are readily available, enabling in situ doping of the as-deposited films. The CVD process, by its very nature, lends itself well to implementation in large-scale reactors. Commercial low-pressure CVD systems, for instance, can typically accommodate loads in excess of 50 wafers, with wafer diameters up to 200 mm. These attributes form the basis for the claim that MEMS benefits from batch fabrication.

The CVD processes used to produce semiconductors and dielectrics in MEMS are, for the most part, those developed originally for the integrated circuit industry or are close variations of such processes. The general CVD process involves the following key steps: (1) transport of precursors to the substrate surface; (2) surface processes that include adsorption of precursors, dissociation of precursors into reactants, migration of reactants to reaction sites, and reactions; and (3) desorption of reaction byproducts from the substrate surface. An explicit mathematical treatment of the CVD process in terms of these steps would be unnecessarily complex for most applications. Fortunately a much less complex, but no less accurate method to quantify the process has been developed.

Known as the Deal–Grove model for CVD growth, this model views CVD growth in terms of two fluxes, namely: a flux of reactants through the boundary layer to the substrate surface, and a flux of reactants involved in film-forming reactions. The first flux is proportional to the difference in reactant concentration across the boundary layer by a proportionality constant known as the mass transfer coefficient. The second flux is also linear to first order with respect to the concentration of reactants at the surface by a constant known as the reaction rate coefficient. Under steady-state conditions (i.e., normal reactor operating conditions) the two fluxes are equal. As such, the lower flux will necessarily govern the process.

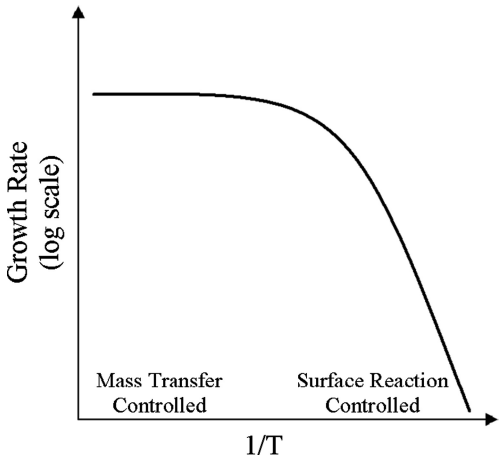

Fig. 2.2 Growth rate versus inverse temperature for a typical CVD process

Figure 2.2 presents an Arrhenius plot of growth rate versus inverse temperature for a representative CVD process.

The process can be divided into two distinct regions based on temperature. At relatively high temperatures, the process is in the mass transfer controlled regime and the process is governed by the flux of reactants through the boundary layer. The boundary layer thickness is generally held constant by way of well-controlled reactor geometries, therefore the growth rate varies relatively slowly with increasing temperature because the mass transfer coefficient is relatively constant with temperature over the temperature range of relevance for CVD. At moderate temperatures, both fluxes influence the deposition rate and thus control of the process is challenging. At relatively low temperatures, the process is described as being in the reaction controlled regime and surface reactions govern the process. In this regime, the growth rate is much more sensitive to temperature because the reaction processes are highly sensitive to temperature. CVD process recipes are generally designed to operate well within either the mass transport controlled regime or the reaction controlled regime as determined primarily by the temperature range required to produce the desired film. Arguably the best example to illustrate this point is the deposition of silicon films. If a single crystalline film is desired, a high-deposition temperature is necessary to initiate epitaxial growth (see Section 2.4 for details) and thus a CVD process in the mass transfer controlled regime is selected. Likewise, deposition of polysilicon requires a much lower substrate temperature; therefore a process in the reaction controlled regime is selected.

2.3.1.2 Low Pressure Chemical Vapor Deposition

Figure 2.3 is a schematic diagram of a typical LPCVD reactor used in MEMS fabrication. The reactor consists of a long, horizontal fused quartz reactor tube sized in length and diameter to accommodate large numbers (∼50) of large-area (i.e.,

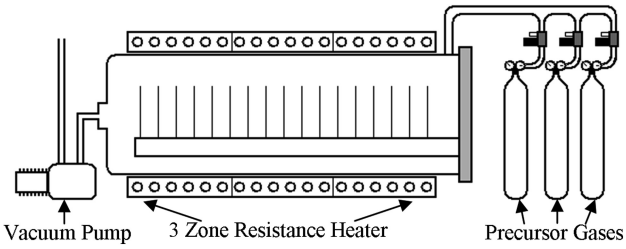

Fig. 2.3 Schematic diagram of a typical large-scale horizontal LPCVD system

200 mm dia.) silicon substrates. End caps with vacuum seals are mounted on each end of the reactor tube to enable operation in the tens to hundreds of mtorr range. The end caps are sometimes water cooled to ensure viable sealing to elastomer o-rings. The contents of the reactor are heated to temperatures up to 1000°C by a large resistive heater that envelops the reactor tube. Precursor gases are introduced via a gas manifold connected to at least one of the end caps. The manifold contains mass flow controllers and associated isolation valves for each precursor gas. The mass flow controllers are calibrated for a specific gas so as to enable precise control of gas flow, which translates to partial pressure of that species in the reactor. Typical flow rates are in standard cc/min (sccm). In addition to the precursor gases, the manifold will also have mass flow controllers for any desired doping gases, inert purge gases, and carrier gases. The process gases may be introduced through a simple port at the end cap or through injector tubes attached to flanges on the end caps that serve to distribute the gases evenly throughout the reactor tube. As mentioned previously, vapors from liquid precursors can be introduced into the reactor by passing the appropriate carrier gas through the source bottle. To maintain the desired deposition pressure, a vacuum system is attached to the end cap opposite the gas injection flanges. The typical vacuum system consists of a large, high-throughput rotary vane pump often assisted by a large roots blower and attached to an end cap through a vacuum line that contains both a pressure control valve and a vacuum isolation valve. The exhaust from the rotary vane pump is fed via a vacuum line to a gas conditioning system which treats the exhaust gas so that it may be safely released.

In general, operation of the aforementioned reactor (commonly called a "furnace" due to its high operating temperatures) follows a procedure that is fairly common for nearly all materials deposited by LPCVD. Prior to loading the furnace, the wafers are cleaned using the standard RCA cleaning procedure described previously. If the wafers have an oxide coating on them, the HF dips in the RCA process are eliminated. Likewise, if the wafers have been metalized, the RCA clean will also be omitted. After cleaning, the wafers are immediately loaded into the furnace by carefully placing them into holders called "wafer boats". Wafer boats are designed to hold the wafers upright and in close proximity to each other so as to maximize the furnace load. The spacing between wafers can be as small as several millimeters. Maintaining uniform deposition with such small spacing between wafers is possible because of the large mean-free path between molecular collisions

at the deposition pressures typically used, which results in a significant increase in diffusivity of precursors with the reactor. The boundary layer thickness increases with decreasing pressure; however, the effect is not nearly as pronounced as the increase in diffusivity. The mass transfer coefficient is proportional to the ratio of gas diffusivity to boundary layer thickness; therefore, decreasing the deposition pressure serves to increase the mass transfer coefficient, thus enabling uniform deposition.

LPCVD processes are typically performed at temperatures between 400 and 900°C in part because it is in this temperature range that good vacuum sealing can be maintained in the large-volume furnaces. One notable exception is epitaxy, where vacuum sealing is maintained for systems operating at temperatures in excess of 1500°C, but these systems are smaller in scale so that the vacuum seals can be kept cool. In the 400–900°C temperature range, the LPCVD furnace operates in the surface reaction controlled regime. In this regime, even small changes in temperature can have a measurable effect on deposition rate (see Fig. 2.2). Fortunately, large-scale furnaces have very large thermal masses, making it relatively easy to hold the reactor at a fixed temperature during film deposition. Operation at these temperatures typically translates to lower surface mobilities for reactant atoms as compared with epitaxial growth temperatures. This tends to promote three-dimensional film growth as a result of nucleation of adsorbed reactants, leading to the formation of amorphous and polycrystalline films. Fortunately, these films have properties needed for a wide range of MEMS devices, therefore eliminating the need for single crystalline films which are much more challenging to deposit.

Maintaining steady-state conditions in large-scale LPCVD reactors is critically important but fortunately relatively easy to achieve. Once the reactor is loaded and has reached the deposition temperature, precursor and doping gases (if desired) are introduced into the reactor at their prescribed flow rates through mass flow controllers that maintain constant flow. Proper vacuum pressure is maintained by adjusting the pressure control valve of the vacuum system. This valve adjusts the conductance in the vacuum line which effectively modulates the gas throughput in the reactor. For a fixed input flow and vacuum system pumping speed, decreasing the conductance leads to an increase in reactor pressure and vice versa. Rarely is input gas flow used as the primary means to control reactor pressure; however, absolute flow rates usually have to be adjusted with respect to the pumping speed of the vacuum system so as to achieve the desired chamber pressure.

For a typical deposition run, temperature, flow rates, and reactor pressure are held constant until the desired film is deposited, after which the gas flows are stopped, the reactor is cooled, and wafers unloaded. Although in principle multiple materials (i.e., polysilicon and silicon nitride) could be deposited using a single reactor, standard practice is to dedicate a reactor to a particular material, if not a particular recipe. This is because LPCVD reactors require “seasoning” in order to produce films with very low run-to-run variation in film properties. Seasoning typically involves the formation of a coating on the interior components of the reaction chamber. The coating, which typically consists of the same material as the deposited film, affects the thermal characteristics of the furnace tube. The coating can also affect the size

of the gas inlet orifices. For any given furnace, there typically is an optimum thickness range for this coating, below which the properties of the as-deposited film vary significantly between runs as well as location in the furnace and above which the coating becomes too thick to withstand thermal and mechanical shock and begins to crack and delaminate, resulting in particulate contaminants in the chamber. Limiting furnace use to a single material and thus restricting the coating to a single material, the thickness range for the coating can usually be extended, thus increasing reactor throughput.

Throughput issues aside, coating composition can affect the properties of the as-deposited film by a process known as autodoping. A form of cross-contamination, autodoping occurs when chemical impurities associated with reactor components are vaporized and incorporated into the deposited film. Autodoping is not a significant factor when a furnace is used to deposit a single material, inasmuch as the source and the deposited film are of the same chemical composition. The same may not be true for a furnace used to deposit multiple materials. Autodoping is even a risk in reactors equipped to deposit intentionally doped films. In the case of polysilicon, fabrication facilities interested in minimizing the risk of autodoping will have dedicated furnaces for both doped and undoped polysilicon.

2.3.1.3 Plasma-Enhanced Chemical Vapor Deposition

Figure 2.4 is a schematic diagram of a typical PECVD reactor. Like its LPCVD counterpart, a PECVD reactor consists of a vacuum chamber, vacuum pumping system, and gas manifold. The gas manifold differs very little, if at all, from the systems used in LPCVD reactors except perhaps for the gases to be used. Both liquid and gaseous precursors are used in PECVD processes. In large part, PECVD systems are used to deposit dielectric films such as silicon oxide and silicon nitride; however, amorphous and polycrystalline semiconductors like silicon can also be deposited. In these cases, doping gases are used to modify conductivity. The vacuum pumping system also closely resembles the LPCVD system, consisting of vacuum valving, gauging, a roots blower, and mechanical rotary pump, and are operated in the same manner.

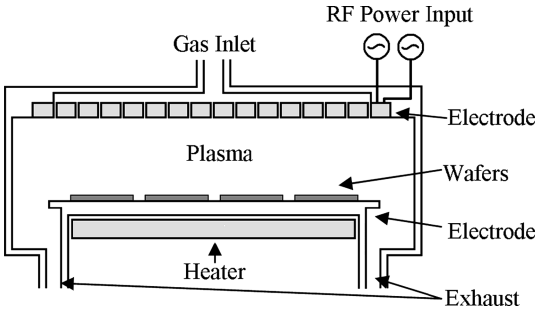

Fig. 2.4 Schematic diagram of a typical PECVD system

The main distinguishing features of the PECVD system can be found inside the vacuum vessel. Unlike the typical LPCVD system, the common PECVD reactor utilizes a stainless steel containment vessel. This is because sample heating is performed by an internal resistive heater that is connected directly to the substrate mounting stage, as opposed to LPCVD which uses an externally mounted resistive heating element. With this configuration, thermal conductivity and thermal mass issues associated with the vacuum vessel are much less a factor and thus stainless steel can be used. In addition to the heater, the vacuum vessel contains two large-area electrodes that are used to generate a plasma inside the chamber. The plasma is generated by connecting the substrate mounting stage to ground and the other electrode to an RF power supply. The RF power supply typically functions at 13.56 MHz and enables the formation of the high electric field required of the plasma.

The plasma is comprised of free electrons, energetic ions, neutral molecules, free radicals, and other ionized and neutral molecular fragments that originate from the precursor gases which are fed at prescribed flow rates from the manifold into the vacuum vessel. In the plasma, high-energy electrons interact kinetically with the precursor gases, causing them to dissociate into the aforementioned components. A film is formed on the wafer as these components are adsorbed on the surface. As with any successful CVD process, these adsorbates migrate to reaction sites where they undergo chemical reactions with other species to form a film. The concentration and composition of free radicals are particularly important because they are highly reactive as a result of having unsatisfied chemical bonds.

The film-forming process is influenced by bombardment of the wafer surface by ions and electrons that are accelerated by the electric field. The plasma supplies a significant source of nonthermal energy, which allows for film deposition to occur at much lower temperatures than would be required if conventional LPCVD were used, a significant advantage when thin film coatings for passivation or chemical or mechanical protection of environmentally sensitive structures are required. Unlike LPCVD processes, which are typically performed at temperatures between 400 and 900°C, typical standard PECVD processes are rarely performed above 400°C. In fact, most standard substrate heaters for PECVD systems have a maximum operating temperature of 400°C, although custom heaters can go much higher in temperature.

The low deposition temperatures, combined with the more complicated film formation processes (i.e., ion bombardment), result in films that exhibit an extremely high sensitivity to deposition parameters. For instance, commonly used precursors either contain hydrogen in their molecular structure or rely on hydrogen as a carrier gas for delivery into the vacuum vessel. The substrate temperatures associated with PECVD can be so low that hydrogen-containing reaction products, including hydrogen itself, cannot desorb from the substrate surface and instead become incorporated into the films. Incorporation of hydrogen results in films with a lower mass density than their stoichiometric counterparts. Under typical processing conditions, it is straightforward to produce films with hydrogen concentrations in excess of 30 at.%. Incorporation of hydrogen also affects the mechanical and optical properties of the as-deposited films in ways that are impossible to generalize but are well documented in the literature.

As-deposited films, especially silicon and its derivatives, are amorphous when deposited by PECVD, but in the case of semiconductors such as silicon and silicon carbide, can be transformed into nanocrystalline films by a postdeposition annealing step. Likewise, a modest postdeposition annealing step at temperatures above 400°C can be effective in modifying the residual stress as-deposited films. These anneals do not induce crystallization, but they are high enough in temperature to initiate densification by hydrogen evolution.

In terms of reactor usage, care must be given to ensure that the as-deposited films are free of pinhole defects. The most significant contributor to pinholes is particulate contamination either by gas phase nucleation or by degradation of coatings on reactor components. Unlike conventional LPCVD, PECVD reactors typically utilize a horizontal configuration where the substrates rest atop the grounded electrode. This geometry lends itself very well to particulate contamination. Mitigation procedures include regular chamber cleaning and proper chamber seasoning. Although cross-contamination is a real concern, most fabrication facilities allow multiple materials to be deposited in the same reactor and many commercially available reactors come equipped for this capability. In these cases, regular chamber cleaning is essential. Fortunately, most vacuum vessels utilize a clamshell design that facilitates easy access to the interior of the reaction chamber and its internal components.

2.3.1.4 Atmospheric Pressure Chemical Vapor Deposition

Simply put, APCVD is a CVD process that is performed at atmospheric pressure. As such, APCVD does not require active pressure control during operation, and thus is well suited for epitaxial growth of single crystalline Si, SiC, and other processes that require high substrate temperatures. Figure 2.5 is a schematic diagram of an APCVD reactor developed for silicon carbide growth. The reactor, which can be horizontally or vertically oriented, consists of a reaction vessel made from a fused quartz, double-walled tube in which water is circulated for cooling. Induction coils connected to an RF generator traverse the circumference of the reaction vessel. Substrates are mounted to an inductively heated, wedgelike susceptor as shown in Fig. 2.5. Precursor gases are mixed with a carrier gas that is delivered at high flow rates, often in the standard liter/min range (slm). The high flow rates serve to reduce the thickness of the boundary layer that forms at the surface of the substrates,

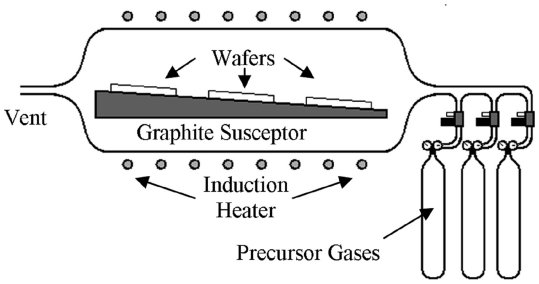

Fig. 2.5 Schematic diagram of a horizontal APCVD reactor

thus enhancing the flux of precursors to the wafer surface. Because of the relatively thick boundary layer, the process is performed in the mass transfer limited regime. High deposition temperatures ensure that surface reactions are not the rate limiting step. As implied by Fig. 2.2, film growth rates are substantially higher than the typical LPCVD process, but precursor depletion effects ultimately limit the number of substrates that a typical reactor can accommodate. Taking into account reactor preparation times, throughput is usually much lower than for the large-scale LPCVD systems, and therefore APCVD is not typically used to deposit polycrystalline and amorphous films for MEMS with the notable exceptions of silicon carbide and thick polysilicon (>10 μm), known as epi-poly, which are featured later in this chapter.

2.3.1.5 Hot Filament Chemical Vapor Deposition

Used primarily as a means to deposit polycrystalline diamond, HFCVD is a special case of LPCVD in which a heated tungsten filament is placed in close proximity to a heated substrate. For diamond growth, the purpose of the filament is to facilitate dissociation of hydrogen gas into atomic hydrogen, which is critical to the preferential formation of diamond over other forms of carbon. For other materials, the hot filament aids in the dissociation of precursor gases, enabling the substrate temperature to be kept lower than in conventional LPCVD. Reliance on the hot filament makes scaleup of HFCVD reactors challenging. HFCVD has also been used to deposit amorphous silicon at temperatures in the 200–300°C range [8–12].

2.3.1.6 Microwave Plasma Chemical Vapor Deposition

A variant of PECVD where instead of using parallel electrodes to generate an electric field at 13.56 MHz, the system is equipped with a microwave source that operates at 2.45 GHz. This method is commonly used in the deposition of polycrystalline, nanocrystalline and ultrananocrystalline diamond films.

2.3.2 LPCVD Polycrystalline Silicon

2.3.2.1 Material Properties and Process Generalities

For both MEMS and IC applications, polycrystalline silicon (polysilicon) films are most commonly deposited by LPCVD. Typical processes are performed in large-scale, horizontal furnaces at temperatures ranging from 580 to 650°C and pressures from 100 to 400 mtorr. The most commonly used source gas is silane (SiH_4). The microstructure of polysilicon thin films consists of a collection of small grains whose microstructure and orientation is a function of the deposition conditions [13]. For typical LPCVD processes (e.g., 200 mtorr), the amorphous-to-polycrystalline transition temperature is about 570°C, with polycrystalline films deposited above the transition temperature. At 600°C, the grains are small and equiaxed, whereas

at 625°C, the grains are large and columnar [13]. The crystal orientation is predominantly (110) Si for temperatures between 600 and 650°C, whereas the (100) orientation is dominant for temperatures between 650 and 700°C.

Although polysilicon can be doped by solid source diffusion or ion implantation, in situ doping during the LPCVD process is an effective means of modifying the electrical properties of the film. In situ doping of polysilicon is performed by simply including a dopant gas, usually diborane (B_2H_6) or phosphine (PH_3), in the CVD process. The inclusion of boron generally increases the deposition rate of polysilicon relative to undoped films, whereas phosphorus reduces the rate [14]. Inclusion of dopants during the LPCVD process leads to the production of conductive films with uniform doping profiles without the high-temperature steps commonly associated with solid source diffusion or ion-implantation. In situ doping is commonly used to produce conductive films for electrostatic devices, but has also been used to create polysilicon-based piezoresistive strain gauges, with gauge factors as high as 15 having been reported [15].

The thermal conductivity of polysilicon is a strong function of its microstructure, which, in turn is dependent on deposition conditions [13]. For fine-grain films, the thermal conductivity is about 25% of the value of single-crystal Si. For thick films with large grains, the thermal conductivity ranges between 50 and 85% of the single-crystal value.

Like the electrical and thermal properties of polysilicon, the as-deposited residual stress in polysilicon films depends on microstructure. For films deposited under typical conditions (200 mtorr, 625°C), the as-deposited polysilicon films have compressive residual stresses. The highest compressive stresses are found in amorphous Si films and in highly textured (110) oriented polysilicon films with columnar grains. Fine-grained polysilicon tends to have tensile stresses. The density of polysilicon has been reported as $2.25 - 2.33\,\mathrm{g/cm^3}$ under varied conditions [16]. The refractive index of polysilicon has been reported as $3.22 - 3.40$ also under varied conditions [16]. The fracture toughness of polysilicon has been measured to be $1.2 \pm 0.2\,\mathrm{MPa}\sqrt{\mathrm{m}}$ [17].

From both the materials properties and processing perspectives, polysilicon has matured to the point that commercial foundries are able to offer full service surface micromachining processes based on LPCVD polysilicon, the two most notable being the MEMSCAP MUMPs^{TM} process and the Sandia SUMMiT V^{TM} process. The MUMPs^{TM} process is a popular multiuser process whose design guidelines can be found in [18]. Although the exact growth conditions of these films are not typically published in the literature, it has been reported that the films are deposited using silane gas at a temperature of 580°C and pressure of 250 mtorr [19]. High-cycle fatigue testing of these films was explored in [20]. Table 2.5 details some of the important material properties that have been reported for the MUMPs^{TM} polysilicon.

Another multiuser process is the Sandia SUMMiT V^{TM} process. This process provides the MEMS designer with five low stress polysilicon structural layers whose conductivity is reported to be $9.10 \pm 0.23 - 33.99 \pm 5.14\,\Omega/\mathrm{sq}$. The complete design guidelines for this process can be found in [23].

Table 2.5 Material properties of polysilicon from the MEMSCAP MUMPs™ process as reported in the literature

References	Thickness (μm)	Young's modulus (GPa)	Poisson's ratio	Tensile strength (GPa)	Residual stress (MPa)	Sheet resistance (Ω/sq)
[21]	3.5	169 ± 6.15	0.22 ± 0.011	1.20 ± 0.15		
[22]	2	149 ± 10			-3.5 ± 0.5	
[18]	$0.5 - 2$	158 ± 10	0.22 ± 0.01	$1.21 - 1.65$	$-50 - 0$	$1 - 45$
[19]	2	162 ± 4	0.20 ± 0.03			

2.3.2.2 Process Selection Guidelines

Many device prototyping facilities that specialize in silicon surface micromachining utilize commercially available, large-scale LPCVD furnaces of the type described previously. From the processing perspective, most of the commercially available furnaces are similar in construction; therefore to first order, process parameters such as furnace temperature, precursor flow rates, furnace pressures tend to fall into fairly narrow ranges. Unfortunately, most process-oriented publications fail to provide details pertaining to the deposition hardware used in the production of the polysilicon films. As a point of reference for readers interested in examining the relationship between furnace hardware and deposition recipes, Table 2.6 details the standard LPCVD polysilicon processes offered by the Microfabrication Laboratory at CWRU. The lab is equipped with two large-scale MRL Industries™ Model 1118 LPCVD furnaces configured specifically for polysilicon, one for undoped polysilicon and the other for in situ phosphorus-doped polysilicon. Each furnace accommodates a 1.93 m long, 235 mm diameter quartz tube.

Table 2.6 LPCVD polysilicon deposition recipes for the two MRL industries™ model 1118 polysilicon furnaces in the microfabrication laboratory at CWRU

Film type	Temp (°C)	Gas	Gas flow (sccm)	Pressure (mtorr)	Dep. rate (nm/min)	Thickness (μm)	Residual stress (MPa)
Undoped	615	SiH_4	100	300	8.5	2	–220
Doped	615	SiH_4	100	300	5.5	2	–150
		PH_3	5				

Examination of the literature reveals that the preponderance of the work in developing LPCVD-based deposition processes for polysilicon MEMS has focused on characterizing the mechanical and electrical properties of the films. Tables 2.7–2.19 summarize a survey of the literature in this area. Tables 2.7, 2.9, 2.10, 2.11, 2.12, and 2.19 focus on undoped polysilicon and Tables 2.8, 2.13, 2.14, 2.15, 2.16, 2.17, 2.18, and 2.19 centern on doped films. Inasmuch as annealing is an important processing step for stress modification and dopant activation, Tables 2.11, 2.12, 2.13, 2.14, 2.15, 2.16, 2.17, 2.18, and 2.19 are specific to annealed films.

Table 2.7 Deposition conditions for undoped LPCVD polysilicon films

References	Temp (°C)	Gas	Gas flow (sccm)	Pressure (mtorr)	Thickness (μm)	Dep. rate (Å/min)
[24]	560–630	SiH_4	30	300–550	2	
[25]	570	SiH_4	100	300	2	45
[26]	570	SiH_4	80	150	1.3	30
[27]	570	SiH_4	45	150		26
[28]	575	SiH_4	43	150	0.25–0.28	30
[27]	580	SiH_4	45	150		30
[29]	580	SiH_4	500	1000		87
[30]	580	SiH_4		300	2 ± 0.02	50
[31]	585	SiH_4	50	200	0.5	40
[27]	590	SiH_4	45	150		35.5
[32, 33]	600	SiH_4	125	550	0.1	
[27]	600	SiH_4	45	150		42
[34]	605	SiH_4	250	550	2	
[35]	605	SiH_4	125	550		100
[27]	610	SiH_4				49
[25]	615	SiH_4	100	300	2	83
[36]	620	SiH_4	70	100	0.46	
[37]	620	SiH_4	70	300	0.5	
[38]	625	SiH_4		250	0.25–1	100
[26]	625	SiH_4	80	180	3	100
[39]	630	SiH_4	20	400	0.2	
		N_2	110			
[40]	635	SiH_4		150	1.5–2	
[41]	640	SiH_4		600	0.23–2.3	100

2.3.2.3 Case Studies

It is generally the case that for LPCVD polysilicon films, the deposition rate increases with increasing temperature. Figure 2.6 is a plot of deposition rate versus deposition temperature for an LPCVD process where the pressure was fixed at 150 mtorr and the SiH_4 flow rate was held constant at 45 sccm [27]. The temperature range examined in this study was from the amorphous-to-polycrystalline transition temperature of roughly 570–610°C, where highly textured, columnar (110) oriented polysilicon is typically deposited. The data illustrate the dramatic increase in deposition rate as a result of the high growth rates associated with (110) Si grains in this temperature range as compared with other orientations. These data show the strong connection between deposition rate and film microstructure in LPCVD polysilicon, an effect that should be taken into account by the process engineer when selecting a particular process route.

Residual stresses in as-deposited polysilicon are heavily dependent on deposition temperature. Figure 2.7 is a plot typical of residual stresses in as-deposited polysilicon films [24]. This figure graphs residual stress versus deposition temperature for polysilicon films deposited at fixed SiH_4 flow rate and three distinct

Table 2.8 Deposition conditions for in situ doped LPCVD polysilicon films

References	Temp (°C)	Gas	Gas flow (sccm or ratio)	Pressure (mtorr)	Thickness (μm)	Dep. rate (Å/min)
[42]	560–610	SiH_4	100	375–800	2	22–83
		PH_3/SiH_4	1.4×10^{-4} to 1×10^{-2}			
[43]	560	SiH_4	100	800	2	
		PH_3	0.16			
[29]	580	SiH_4	500	1000		45
		PH_3/SiH_4	10×10^{-3}			
[43]	590	SiH_4	50	500	2	
		PH_3	0.16			
[43]	610	SiH_4	100	375	2	
		PH_3	1			
[44]	625	SiH_4	60	750	0.4	46.25
		PH_3	30			
		N_2	300			
[45]	650	PH_3/SiH_4	1:99	320	0.1–2	26.7
[46]	555	SiH_4	200–400	350		24–105
		BCl_3 [a]	0–180			

[a] 3% in N_2

Table 2.9 Mechanical properties of undoped LPCVD polysilicon films

References	Temp (°C)	SiH_4 flow (sccm)	Pressure (mtorr)	Thickness (μm)	Young's modulus (GPa)	Tensile strength (GPa)	Fracture toughness (MPa$\sqrt{m}$)
[47]	565			1		2.84 ± 0.09	
[48]	580			2.1	175 ± 21		
[17]	580			3.5			1.2 ± 0.2
[49]	620			1–1.4	175 ± 25	2.7–3.4	
[36]	620	70	100	0.46	151 ± 6		
[36]	620	70	100	0.46	162 ± 8		
[39]	630	20[a]	400	0.2	160		
[50]	630	na[b]		4	190		

[a] N_2 gas at 110 sccm also used during deposition
[b] H_2 gas also used during deposition

deposition pressures. The residual stresses are compressive regardless of deposition pressure for temperatures below 580°C. At a temperature of 600°C, the residual stress is moderately or highly tensile, but transitions dramatically back to compressive for a deposition temperature of 620°C. These observations correlate strongly to the varying microstructure in polysilicon films over this relatively small temperature range.

Figure 2.7 above illustrates the difficulty in using deposition parameters to control the residual stress in as-deposited polysilicon films. Fortunately, postdeposition

Table 2.10 Residual stress in as-deposited, undoped LPCVD polysilicon films

References	Temperature (°C)	SiH_4 flow (sccm)	Pressure (mtorr)	Thickness (μm)	Residual stress (MPa)
[24]	560–630	30	300–550	2	–340 to 1750
[26]	570	80	150	1.3	82
[25]	570	100	300	2	270
[32, 33]	600	125	550	0.1	12
[25]	615	100	300	2	–200
[25]	570–615	100	300	2.72	<10[a]
[36]	620	70	100	0.46	-350 ± 12
[39]	630	20[b]	400	0.2	–180

[a]The stress gradient in this film is $\leq$2 MPa/μm
[b] N_2 gas at 110 sccm also used during deposition

Table 2.11 Residual stress in undoped LPCVD polysilicon films subjected to post deposition annealing

References	Deposition temperature (°C)	SiH_4 flow (sccm)	Pressure (mtorr)	Annealing conditions	Thickness (μm)	Residual stress (MPa)
[47]	565			1050°C, 10 s RTA[a]	1	142
[26]	570	80	150	1200°C, 6 h	1.3	17
[25]	570	100	300	1100°C, 30 min	2	30
[17]	580			1000°C, 1 h	3.5	12 ± 5
[31]	585	50	200	650°C, 3 h[b]	0.5	250
[25]	615	100	300	1100°C, 30 min	2	–20
[37]	620	70	300	900–1150°C, 1–10 s RTA	0.5	–340 to 90
[36]	620	70	100	1100°C, 2 h	0.46	Low stress
[26]	625	80	180	1200°C, 6 h	3	–205
[50]	630	Dna[c]		1000°C, 90 min	4	42

[a]RTA: Rapid Thermal Anneal
[b]Anneal performed at 500 mtorr
[c]H_2 gas also used during deposition

annealing is an effective means to alter the residual stress in as-deposited polysilicon films. Temperatures required for effective stress modification (~1000°C) are easily achievable. For example, it has been reported that residual stresses of about –500 MPa can be reduced to less than –10 MPa by annealing at 1000°C in a N_2 ambient [55, 56]. If performed in a conventional furnace, such high-temperature annealing could be problematic if the substrate contains temperature-sensitive elements such as selectively doped regions. Fortunately, rapid thermal annealing has proven to be an effective method of stress reduction in polysilicon films. It has been reported that a 10 s anneal at 1100°C was sufficient to completely relieve the stress

Table 2.12 Strain in undoped LPCVD polysilicon films subjected to postdeposition annealing

References	Temp. (°C)	SiH_4 flow (sccm)	Pressure (mtorr)	Annealing conditions	Thickness (μm)	Residual strain
[28]	575	43	150	600°C	0.25–0.28	~600 μstrain (tensile)
[48]	580			1000°C, 2 h 1050°C, 3 h	2.1	0.021–0.0084%
[30]	580		300	600°C, 180 min	2	–0.001 to 0.7% (comp)
[34]	605	250	550	950°C, 2 h	2	0.017% (tensile)
[40]	635		150		1.5–2	0.01%

Table 2.13 Mechanical properties of in situ doped LPCVD polysilicon films

References	Temp (°C)	SiH_4 flow (sccm)	Pressure (mtorr)	Doping and annealing conditions	Thickness (μm)	Young's modulus (GPa)
[43]	560	100	800	PH_3 at 0.16 sccm, 1050°C, 10 s RTA[a]	2	147 ± 2.4
[43]	590	50	500	PH_3 at 0.16 sccm, 1050°C, 10 s RTA	2	153 ± 2.8
[43]	610	100	375	PH_3 at 1 sccm, 1050°C, 10 s RTA	2	130 ± 3.9
[51]	650			Heavily P-doped	1.27	123

[a]RTA: Rapid Thermal Anneal

in films with an as-deposited stress of about –340 MPa [37]. Rapid thermal processing has even been used as the primary heat source in polysilicon LPCVD [57], offering a high-throughput, low thermal budget alternative to conventional LPCVD for applications where a thin polysilicon layer may be required on preprocessed wafers, such as polysilicon-based piezoresistors.

Figure 2.8 shows the relationship between residual stress and annealing temperature for films deposited at 550, 570, 580, and 615°C [25]. For this dataset, each anneal was each performed for 30 min in N_2. From a processing perspective, these data show that regardless of the as-deposited stress, residual stresses near zero can be achieved for annealing temperatures at or above 1000°C for films that were deposited near the amorphous-to-crystalline transition temperature, and 1100°C for high-textured polysilicon films. An early study showed that high-temperature annealing (~1100°C) resulted in grain growth and recrystallization, regardless of whether the polysilicon was deposited on thermal oxide or LPCVD oxide [56].

Table 2.14 Mechanical properties of LPCVD polysilicon films doped by ion implantation

References	Temp (°C)	Doping and annealing conditions	Thickness (μm)	Tensile strength (GPa)	Young's modulus (GPa)
[47]	565	P, 80 keV, $4.0 \times 10^6 cm^{-2}$, 1050°C 10 s RTA[a]	1	2.11 ± 0.10	
[47]	565	As, 120 keV, $4.0 \times 10^6 cm^{-2}$, 1050°C 10 s RTA	1	2.70 ± 0.09	
[47]	565	B, 15 keV, $2 \times 10^{16} cm^{-2}$, 1050°C 10 s RTA	1	2.77 ± 0.08	
[16]	620	Varied implant and annealing conditions	0.1–0.8		151–166

[a]RTA: Rapid Thermal Anneal

Table 2.15 Mechanical properties of LPCVD polysilicon films doped by PSG[a]-based diffusion and unspecified methods

References	Temp (°C)	Pressure (mtorr)	Doping and annealing conditions	Thickness (μm)	Young's modulus (GPa)	Tensile strength (GPa)
[19]	580	250	PSG, 1050°C 1 h	2	1.62 ± 4	
[43]	610		PSG, 1050°C 10 s RTA[b]	2	168 ± 7	
[16]	620	100	Varied doping Varied anneal	0.1–0.8	151–166	
[52]	630		PSG, 1000°C, 1 h	1	169	2–3
[51]	650		Heavily P-doped	1.27	123	

[a]Phosphosilicate glass
[b]RTA: Rapid Thermal Anneal

Reduction in residual stress can be achieved in polysilicon by means other than high-temperature annealing. For instance, a process has been developed that utilizes the residual stress characteristics of polysilicon deposited under various conditions to construct polysilicon multilayers that have the desired thickness and stress values [25]. The multilayers are comprised of alternating tensile and compressive

Table 2.16 Residual stress in doped LPCVD polysilicon films

References	Temp (°C)	SiH_4 flow (sccm)	Pressure (mtorr)	Doping and annealing conditions	Thickness (μm)	Residual stress (MPa)	Stress gradient (MPa/μm)
[42]	560–610	100	375–800	In situ: PH_3 PH_3/SiH_4: $1.4 \times 10^{-4} - 1 \times 10^{-2}$ Anneal: 900°C, 10–120 s RTA[a]	2	–195 to 310	
[53]	580			P implantation: $1 - 4 \times 10^{15}/cm^2$. Anneal: 950°C, 1–10 h	2	40.3–83.9	4.7–29.2
[54]	580		350	P diff. or ion implant, Varied anneal	2	26–72	0.3–24
[31]	585	50	200	$POCl_3$ diffusion: 850–950°C N_2: 2 slm O_2: 100 sccm $POCl_3$: 100 sccm 650°C, 3 h, 500 mtorr	0.5	–110	
[16]	620		100	Varied doping Varied anneal	0.1–0.8	–560 to 30	
[26]	625	80	180	$POCl_3$ diffusion: 1 h at 950–1100°C. Anneal: 1200°C, 6 h	3	–98 to 11	

[a]RTA: Rapid Thermal Anneal

Table 2.17 Electrical properties of in-situ doped polysilicon films

References	Temp (°C)	Gas	Gas flow (sccm or ratio)	Pressure (mtorr)	Dep. rate (Å/min)	Resistivity (mΩ cm)	Annealing
[42]	560–610	SiH_4 PH_3/SiH_4	$100\,(0.014-1)\times 10^{-2}$	375–800	22–83	0.46–5.3	RTA[a] 900°C, 10–120 s
[29]	580	SiH_4	500	1000	45	0.5	980°C, 30 min
		PH_3/SiH_4	0.01				
[44]	625	SiH_4	60	750	46.25	1	900°C, 30 min
		PH_3	30				
		N_2	300				
[46]	555	SiH_4	200–400	350	24–105	0.002–0.03	None
		BCl_3[b]	0–180				
[45]	650	PH_3/SiH_4	0.01	320	26.7	1.7	None

[a]RTA: Rapid Thermal Anneal
[b]3% in N_2

Table 2.18 Electrical properties of LPCVD polysilicon doped by diffusion

Reference	Deposition temperature (°C)	Gas	Flow rate (sccm)	Pressure (mtorr)	Diff. temp. (C)	Sheet resistance (Ω/sq)	Annealing conditions
[31]	585	SiH_4 O_2 N_2 $POCl_3$	50 100 2000 100	200	850–950	12	650°C, 3 h, 500 mtorr

Table 2.19 Surface roughness and refractive index of annealed LPCVD polysilicon

References	Temp (°C)	Gas	Pressure (mtorr)	Thickness (μm)	Dep. rate (Å/min)	Surface roughness (nm)	Refractive index	Annealing conditions
[30]	580	SiH_4	300	2	50	0.8		600°C, 180 min
[25]	615	SiH_4	300	2	83	71		1100°C, 30 min
[16]	620	SiH_4	100	0.1–0.8			3.2–3.4	Varied
[44]	625	SiH_4 PH_3 N_2	750	0.4	46	12		900°C, 30 min

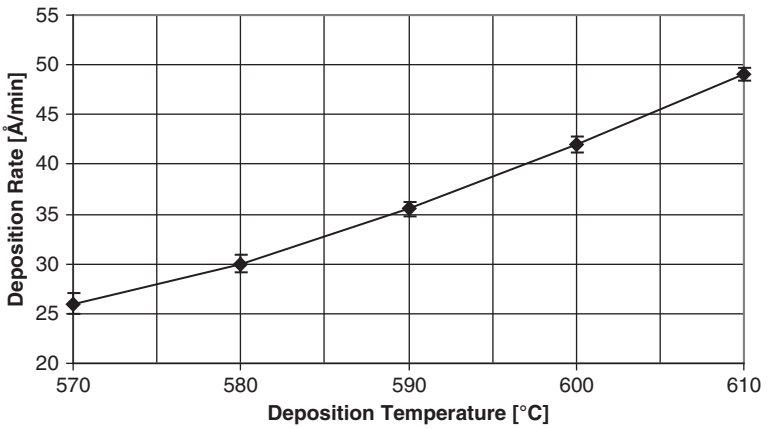

Fig. 2.6 Polysilicon growth rate as a function of temperature for silane gas reacted at 45 sccm and 150 mtorr in a 15 cm diameter horizontal LPCVD furnace [27] (Reprinted with permission. Copyright 2002 Elsevier)

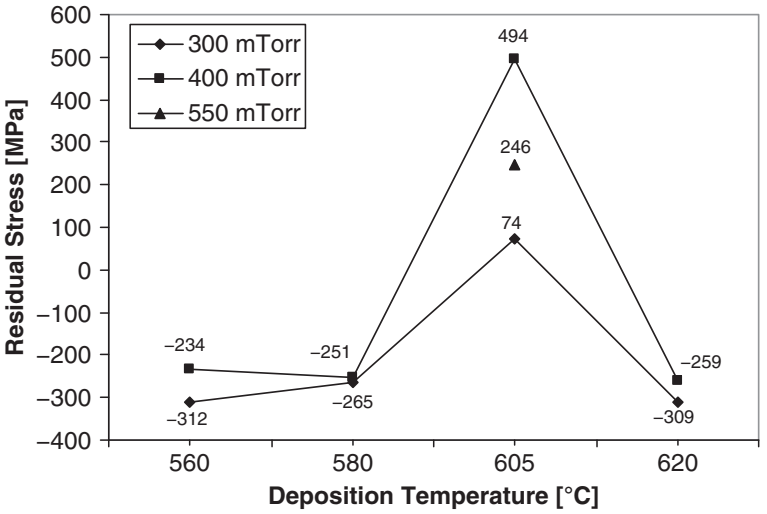

Fig. 2.7 Polysilicon residual film stress as a function of deposition temperature and pressure for 2 μm thick films deposited using silane at 30 sccm [24] (Reprinted with permission. Copyright 2001, Elsevier)

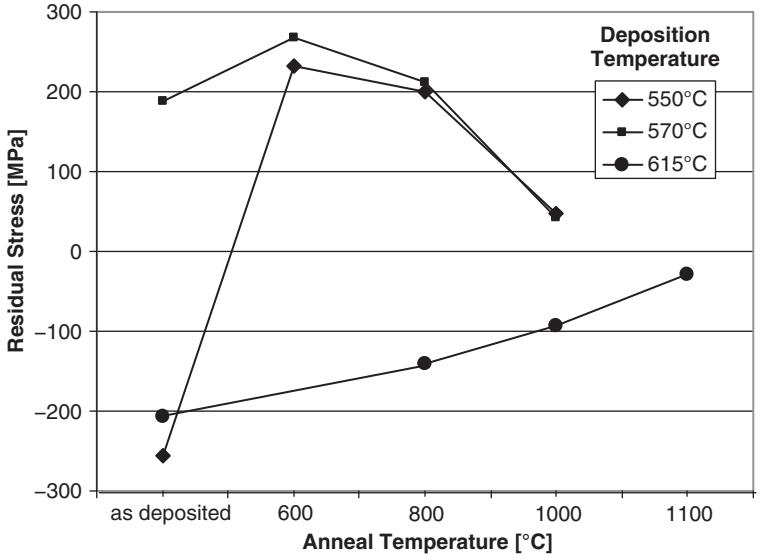

Fig. 2.8 Residual film stress as a function of annealing temperature for 2 μm thick polysilicon films deposited at varied temperatures and annealed for 30 min in N_2 [25] (Reprinted with permission. Copyright 2000 IEEE)

polysilicon layers that are deposited in a sequential manner. Known as the "multipoly process," the tensile layers consist of fine-grained polysilicon grown at a temperature of 570°C, and the compressive layers are made up of columnar polysilicon deposited at 615°C. The overall stress in the composite film depends on the number of alternating layers and the thickness of each layer. With the proper selection of layer thickness, a polysilicon multilayer can be deposited with near-zero residual stress (<10 MPa) and very little stress gradient (<0.2 MPa/μm) in a ten-layer stack. The process does not require annealing, a considerable advantage for MEMS fabrication processes with restricted thermal budgets.

Along similar lines, nickel silicide (Ni_xSi_y) films have been used to compensate for residual stress gradients in polysilicon thin films [58]. Silicides are used in CMOS technology to reduce sheet and contact resistances in polysilicon gates and thus are compatible with polysilicon MEMS processing. Silicide films are formed on polysilicon surfaces by depositing a Ni film by thermal evaporation and annealing the film at ~400°C. The resulting sheet resistance is reduced from 20,000 to 10 Ω/sq; and the stress gradient is completely eliminated by annealing at 290°C.

2.3.3 LPCVD Silicon Dioxide

2.3.3.1 Material Properties and Process Generalities

Like its thermally grown counterpart, SiO_2 deposited by LPCVD is an electrical insulator. The dielectric constant of LPCVD SiO_2, commonly referred to as LTO or low temperature oxide due to its low deposition temperature when compared to thermal oxidation, is 4.3. The dielectric strength of LTO is about 80% of that for thermal oxide [59]. Unlike thermal oxide, the residual stress in LTO is process-dependent and tends to be compressive in as-deposited films.

LPCVD SiO_2 is one of the most widely used materials in the fabrication of MEMS. In polysilicon surface micromachining, LPCVD SiO_2 is used as a sacrificial material because it can be easily dissolved using etchants that do not attack polysilicon. LTO is widely used as an etch mask for dry etching of thick polysilicon films, because it is chemically resistant to dry etching processes for polysilicon. LTO films are also used as passivation layers on the surfaces of environmentally sensitive devices.

LPCVD SiO_2 films can be deposited on a wide variety of substrate materials, including Si, polysilicon, silicon nitride, silicon carbide, and substrates metalized with temperature-tolerant metals. In general, LPCVD provides a means for depositing thick (>2 μm) SiO_2 films at temperatures much lower than thermal oxidation. LTO films have a higher etch rate in HF than thermal oxides, which translates to significantly faster release times when LTO films are used as sacrificial layers. Phosphosilicate glass (PSG) can be formed using nearly the same deposition process as LTO by adding a phosphorus-containing gas to the precursor flows in an in situ doping process that resembles in situ polysilicon doping. PSG films are useful as sacrificial layers because they generally have higher etching rates in HF than

LTO films. PSG is compatible with LPCVD polysilicon deposition conditions, thus enabling its use in multilayered polysilicon surface micromachining processes [60]. Polysilicon films deposited at 605°C on PSG sacrificial layers exhibit a strong (111) texture and very low residual strains ($< 5 \times 10^{-5}$) [61], which are in stark contrast to similar films deposited on thermal oxide and LTO, which have high residual strains ($\sim -3 \times 10^{-3}$) and are highly textured (110) oriented films. The difference may be attributed to the influence of phosphorous on nucleation and grain growth in polysilicon.

PSG has been used as a source of dopants for LPCVD polysilicon films [18]. The process simply involves cladding an undoped polysilicon layer between two PSG layers and annealing the structure at 1050°C in N_2. The annealing step serves to drive phosphorus dopant atoms into the polysilicon from both top and bottom surfaces simultaneously, which dopes the films and balances the residual stresses. PSG layers as thin as 300 nm can be used to dope 1.5 μm thick polysilicon with phosphorus to a resistivity of 0.02 Ω cm [62]. Anneals for doping purposes can be performed at temperatures above 1100°C, however, concerns over delamination of PSG from underlying silicon nitride layers cap the annealing at 1050°C [63].

PSG and LTO films are deposited in hot-wall, low-pressure, fused silica furnaces in systems similar to those described previously for polysilicon. Precursor gases include SiH_4 as a Si source, O_2 as an oxygen source, and, in the case of PSG, PH_3 as a source of phosphorus. The single-source precursor tetraethoxysilane (TEOS or $Si(OC_2H_5)$) is also used to deposit oxides by LPCVD, albeit at higher deposition temperatures (~700°C). Silane-based LTO and PSG films are typically deposited at temperatures of 425–450°C and pressures ranging from 200 to 400 mtorr. The low deposition temperatures result in LTO and PSG films that are slightly less dense than thermal oxides due to the incorporation of hydrogen in the films. LTO films can, however, be densified by an annealing step at high temperature (1000°C). The low mass density of LTO and PSG films is partially responsible for the increased etch rate in HF. It has been found that the residual stress in PSG is about 10 MPa for phosphorus concentrations of 8% [64]. LTO and PSG films conform to undulant topographies, however, the degree of conformation is affected by low surface migration associated with the low deposition temperatures. PSG will reflow at temperatures above 900°C, a characteristic that can be used to alter coating thicknesses and profiles on undulant topographies.

2.3.3.2 Process Selection Guidelines

A review of the literature reveals that efforts to develop LTO and PSG beyond their roles as sacrificial, etch mask, bonding, and passivation materials are very rare. As a consequence, the literature lacks the wealth of information linking process conditions to material properties that can easily be found for structural materials such as polysilicon, silicon nitride, and silicon carbide. Although many surface micromachined MEMS devices are fabricated using LTO and/or PSG in the process sequence, most papers simply mention that these films were used and do not provide details pertaining to their deposition. This is ostensibly due to the fact that in most

Table 2.20 Deposition conditions for LTO and PSG films deposited in the MFL at CWRU

Film type	Temp (°C)	Gas	Gas flow (sccm)	Pressure (mtorr)	Dep. rate (nm/min)	Residual stress (MPa)
LTO	450	SiH_4	51	350	15	∼–150
		O_2	61			
PSG	450	SiH_4	40	350	9.5	∼40
		O_2	60			
		PH_3	37.5			

cases, the films are deposited in large-scale, commercially available systems using vendor-provided recipes that were developed several decades ago for IC processing and thus the properties are common knowledge in the MEMS community.

Because nearly all MEMS fabrication facilities that offer polysilicon surface micromachining have an LPCVD oxide as part of their CVD repertoire, it would be remiss to omit key information regarding the deposition of such films. Table 2.20 details the standard LTO and PSG processes offered by the Microfabrication Laboratory at CWRU. The LTO and PSG deposition processes in this facility are performed in the same furnace platform (MRL Industries™ Model 1118) as previously described for polysilicon. The deposition processes closely resemble those commonly used in MEMS prototyping facilities that are equipped with high-throughput LPCVD furnaces.

LTO and PSG films were initially developed for passivation and intermetal dielectric layers in silicon-based ICs and the body of work in these areas is quite extensive. Reviewing this work is beyond the scope of this chapter, although a few references are worth noting due to their impact on MEMS technology. Tables 2.21, 2.22, and 2.23 summarize the process parameters and resulting material properties of relevance to MEMS from these publications.

Table 2.21 Deposition parameters and material properties for as-deposited PSG films

References	Temp (°C)	Gas	Gas flow ratio	Pressure (mtorr)	Deposition rate (nm/min)	Etch rate in HF (nm/s)	Residual stress (MPa)
[65]	425	O_2/SiH_4	4.35	200	8.0	>7	
		PH_3/SiH_4	0.22				
[66]	425	O_2/SiH_4	2	200	20	5	–10
		PH_3/SiH_4	0.1				
[67]	700	O_2/TEOS	1.23		70	9	200
		PH_3/TEOS	0.19				

2.3.3.3 Case Studies

References [65–67] contain much more information that might be of interest to the MEMS process engineer than are summarized in Tables 2.21, 2.22, and 2.23

Table 2.22 Deposition parameters and material properties for as-deposited LTO films

References	Temp (°C)	Gas	Gas flow ratio	Pressure (mtorr)	Deposition rate (nm/min)	Etch rate in HF (nm/s)	Residual stress (MPa)
[65]	425	O_2/SiH_4	4.35	200	7.5	~0.5	
[66]	425	O_2/SiH_4	2	200	20	0.67	–100
[67]	700	O_2/TEOS PH_3/TEOS	1.23 0.19		70	9	200

Table 2.23 Properties of annealed PSG and LTO films

References	Film	Gases	Deposition temperature (°C)	Annealing time and temperature	Etch rate in HF (nm/s)	Residual stress (MPa)
[65]	PSG	$O_2/SiH_4/PH_3$	425	30 min, 850°C	~6.4	
	LTO	O_2/SiH_4	425	30 min, 850°C	<0.5	
[66]	PSG	$O_2/SiH_4/PH_3$	425	30 min, 600°C		~0
		O_2/SiH_4	425	30 min, 850°C		–20
[67]	PSG	O_2/TEOS/PH_3	700	10 min, 950°C	5	100

and thus the interested reader is urged to seek these papers. For instance, [67] details the optical properties of TEOS-based PSG films and [66] characterizes the absorption coefficient, transmittance, dielectric constant, and breakdown voltage of as-deposited and annealed films. In addition, [66] compares PSG films deposited by LPCVD to those deposited by APCVD and PECVD. With respect to MEMS fabrication, Poenar et al. investigated PSG films specifically for surface micromachining [65]. They reported that the vertical etch rate as well as lateral undercut etch rate increased exponentially with increasing phosphorous content in the films. After annealing, the etch rates decreased by up to 70%, but this was not solely due to phosphorus out-diffusion or densification, but rather other structural changes in the film, such as bond configuration. It was also found that the phosphorous content has little effect on strain in polysilicon structural layers. They concluded that for surface micromachining applications, a PH_3/SiH_4 ratio was optimum for PSG sacrificial etching, yielding an etch rate of 8.5 μm/min in 20% HF with a shrinkage upon annealing of only 6%. In addition to these papers, readers interested in an in-depth review of silicon dioxide sacrificial etching should consider an excellent review by Buhler et al. [68].

2.3.4 LPCVD Silicon Nitride

2.3.4.1 Material Properties and Process Generalities

Silicon nitride (Si_3N_4) is widely used in MEMS for substrate isolation, surface passivation, etch masking, and as an electrically insulating structural material in suspended membranes, bridges, and other related structures owing to its physical properties [1]. Si_3N_4 is extremely resistant to chemical attack with an etch rate in HF of ~1 nm/min, thereby making it the material of choice for surface micromachining applications where oxide is used as a sacrificial layer. Si_3N_4 is commonly used as an insulating layer because it has a resistivity of $\sim 10^{14}$ Ω cm and dielectric strength of 10^7 V/cm. Silicon nitride has an electric bandgap of ~5 eV, which is considerably lower than thermal oxide, but because it has no shallow donors or acceptors, it behaves as an insulator. Silicon nitride is amorphous in microstructure with a mass density of 3.1 g/cm^3.

LPCVD Si_3N_4 films are deposited in horizontal furnaces similar to those used for polysilicon deposition. Typical deposition temperatures and pressures range between 700–900°C and 200–500 mtorr, respectively. The standard source gases are dichlorosilane (SiH_2Cl_2) and ammonia (NH_3). To produce stoichiometric Si_3N_4 a SiH_2Cl_2-to-NH_3 ratio in the range of 1:10 is commonly used. The microstructure of films deposited under these conditions in amorphous.

The residual stress in stoichiometric Si_3N_4 is large and tensile, with a magnitude of about 1 GPa [69]. Such a large residual stress causes films thicker than a few hundred nanometers to crack. Nonetheless, thin stoichiometric Si_3N_4 films have been used as mechanical support structures and electrical insulating layers in piezoresistive pressure sensors [70]. For applications that require micron-thick, durable, and chemically resistant membranes, nonstoichiometric Si_xN_y films can be deposited by LPCVD. These films, often referred to as Si-rich or low-stress nitride, are intentionally deposited with an excess of Si by simply increasing the ratio of SiH_2Cl_2 to NH_3 during deposition. Nearly stress-free films can be deposited using a SiH_2Cl_2-to-NH_3 ratio of 6:1, a deposition temperature of 850°C and a pressure of 500 mtorr [71]. A detailed study concerning the influence of the Si-to-N ratio on the residual stress in silicon nitride films can be found in [72, 73]. The composition of low-stress nitride has been reported to be $Si_{1.0}N_{1.1}$ [74]. The increase in Si content not only leads to a reduction in tensile stress, but also a decrease in the etch rate in HF. Such properties have enabled the development of MEMS structures and fabrication techniques that would otherwise not be feasible with stoichiometric Si_3N_4. For example, low-stress silicon nitride has been bulk micromachined using silicon as the sacrificial material [75]. In this case, Si anisotropic etchants (TMAH) were used for dissolving the sacrificial silicon. Low-stress silicon nitride has also been employed as a structural layer in surface micromachining using PSG as a sacrificial layer [76], capitalizing on the HF resistance of the nitride films.

The strength of silicon nitride films also varies with the Si-to-N ratio. For example, the tensile strength has been reported to be 6.4 GPa for stoichiometric films and 5.5 GPa for silicon-rich films [77]. A similar decrease in fracture toughness is

observed for silicon-rich silicon nitride with an upper bound to be <14 MPa$\sqrt{m}$ for stoichiometric nitride and 1.8 MPa$\sqrt{m}$ for low-stress nitride [78].

2.3.4.2 Process Selection Guidelines

The MFL at CWRU offers both stoichiometric and low-stress silicon-rich silicon nitride films deposited using a MRL Industries^{TM} Model 1118 LPCVD furnace as previously described for polysilicon. Recipe details for these processes are shown in Table 2.24.

Table 2.24 Deposition conditions for stoichiometric and low-stress nitride films deposited at CWRU

Film type	Temp (°C)	Gas	Gas flow (sccm)	Pressure (mtorr)	Dep. rate (nm/min)	Residual stress (MPa)
Stoichiometric	820	DCS[a]	18	280	3	~1000
		NH_3	108			
Si-rich	850	DCS	62.5	~200	1.8	~100
		NH_3	17.5			

[a]DCS = dichlorosilane (SiH_2Cl_2)

Although the deposition rate for low-stress nitride in the CWRU system is lower than that of the stoichiometric nitride, others have reported that for a SiH_2Cl_2-to-NH_3 ratio of 4:1 at 835°C and 300 mtorr, the deposition rate is over twice the rate in the CWRU system at 4 nm/min [45].

Tables 2.24 and 2.25 describe the process-related material properties of LPCVD silicon nitride films. Table 2.25 describes processes with respect to the precursor flow rate and Table 2.26 is based on precursor flow ratio. Table 2.27 details the mechanical properties of annealed silicon nitride films deposited by LPCVD.

2.3.4.3 Case Studies

The chemical resistance of silicon nitride lends itself to the fabrication of very thin membranes by silicon bulk micromachining. Reference [69] describes a study to characterize the mechanical properties of stoichiometric Si_3N_4 using 70–80 nm thick membranes. A 70–80 nm thick Si_3N_4 film was deposited on (100) Si wafers that were coated with a 300 nm oxide film. Rectangular windows were patterned on the backside of the wafer and an anisotropic Si etch was performed, stopping on the thin oxide. A brief hydrofluoric acid etch was then used to dissolve the thin oxide film, revealing 200–600 μm wide by 2400–11000 μm long nitride membranes. Load-deflection testing was then used to characterize the films, yielding a biaxial modulus of 288 GPa, a fracture stress of 10.8–11.7 GPa, and a residual stress of 1040 MPa [69].

As mentioned previously, the high residual stresses found in stoichiometric Si_3N_4 limit its use to very thin films. In surface micromachining, a nitride layer is desirable to isolate devices electrically from the bulk substrate. To prevent wafer warpage

Table 2.25 Mechanical properties of LPCVD silicon nitride[a]

References	Temp (°C)	Gas	Gas flow (sccm)	Pressure (torr)	Thickness (μm)	Young's modulus (GPa)	Residual stress (MPa)
[6]	770	DCS[b]	50	0.25	0.3	305[c]	1132
		NH_3	300				
[39]	790	DCS	20	0.6	0.2	290	1000
		NH_3	170				
[77]	820	DCS	18	0.28	0.2	325	1170–1300
		NH_3	108				
[51, 74]	835	DCS	70	0.3	2.1	373	
		NH_3	15				
[34]	835	DCS	64	0.3	1.5		96
		NH_3	16				
[79]	840	DCS	64		0.5	220	280
		NH_3	16		0.7		360
[80]	850–880	DCS	80–448	0.25–0.6	0.4–2.4		–52 to 641
		NH_3	24–187				
[80]	880	DCS	96	0.6			0 ± 10
		NH_3	24				

[a] With respect to precursor flow rates
[b] DCS: Dichlorosilane (SiH_2Cl_2)
[c] Biaxial modulus

Table 2.26 Mechanical properties of LPCVD silicon nitride[a]

References	Temp (°C)	Gas	Ratio	Pressure (mtorr)	Thickness (μm)	Young's modulus (GPa)	Residual stress (MPa)
[81]	770	DCS[b]/NH_3	0.05–0.5				~1000
[82]	785	DCS/NH_3	0.33	368		330	1020
[5]	800	DCS/NH_3	0.33				860
[83]	850	DCS/NH_3	0.33				1200
[76]	850	DCS/NH_3	0.33	150		320	967
[73]	775	SiH_4/NH_3	0.625	203			600
[73]	750	SiH_4/NH_3	2				<–50
[77]	na	DCS/NH_3	4		0.3	295	322
[71]	850	DCS/NH_3	4	500	2		98
[83]	850	DCS/NH_3	4				<–100
[84]	850	DCS/NH_3	5		1	186	108
[85]	800	DCS/NH_3	5.5	14			1200
[76]	850	DCS/NH_3	5.7	150		360	125
[82]	785	DCS/NH_3	6	368		230	430

[a] With respect to precursor flow ratios
[b] DCS: dichlorosilane (SiH_2Cl_2)

Table 2.27 Mechanical properties of annealed LPCVD silicon nitride films

References	Temp (°C)	Gas	Gas flow (sccm) or ratio	Pressure (torr)	Thickness (μm)	Annealing conditions	Young's modulus (GPa)	Tensile strength (GPa)	Residual stress (MPa)
[86]	840	DCS[a] NH_3	6–1	0.17	0.76	1100°C, N_2 2 h	202	12	291
[87]	840	DCS NH_3 N_2	1000 16 100	0.2	0.3–0.7	1100°C Forming gas 2 h	248		
[83]	850	DCS/NH_3	4			O_2, 1100°C, 3 h			10

[a]DCS = dichlorosilane (SiH_2Cl_2)

due to stress, the stoichiometric silicon nitride is typically left on the backside of the wafer. In order to access the bulk wafer electrically, one must pattern access vias through the nitride layer. The MEMSCAP MUMPS^{TM} process incorporates a 600 nm low-stress nitride film to isolate devices, allowing complete backside nitride removal [18]. In order to characterize the in situ stress of a 1.5 μm thick low-stress nitride film, a microfabricated vernier strain gauge was realized [34]. Deposited at 835°C with a pressure of 300 mtorr using SiH_2Cl_2 and NH_3 flow rates of 64 and 16 sccm, respectively, the stress was measured to be 96 MPa.

Silicon-rich silicon nitride films are attractive for MEMS applications not only for their low residual stresses, but also for their attractive thermal properties. Matrangelo et al. describe a process to measure the thermal conductivity and heat capacity of low stress nitride using microbridge structures [74]. In their study, the authors used a low-stress nitride ($Si_{1.0}N_{1.1}$) deposited at 835°C using SiH_2Cl_2 and NH_3 flow rates of 70 and 15 sccm, respectively. The microbridge fabrication process began with the deposition of a 3 μm phosphosilicate glass layer on a silicon substrate, after which the PSG was annealed for 5 h at 1100°C. Next a 2–4 μm thick low-stress nitride was deposited using the parameters above. A 200–600 nm thick layer of undoped polysilicon was deposited and then heavily doped using PSG. The silicon and nitride layers were then formed into 200 μm long by 3 μm wide bridge structures by reactive ion etching (RIE). The bridges were released by etching away the PSG in HF. Using these bridge structures, the low-stress nitride films were found to have a mass density of 3.0 g/cm^3, a thermal conductivity of 3.2×10^{-2} W/cm K, and a heat capacity of 0.7 J/gK.

Surface micromachined structures have also been used to determine the Young's modulus of low-stress nitride films [51]. In this study, a silicon wafer was first coated with a 4 μm thick PSG layer, followed by the deposition of a 2 μm thick low-stress nitride film. The nitride film was then patterned into microbridges by RIE and a timed etch in buffered HF was used to release the structures. A stylus profilometer was scanned along the length of the microbridges, allowing the Young's modulus to be extracted. The Young's modulus in the $Si_{1.0}N_{1.1}$ films was found to be 373 GPa [51].

2.3.5 LPCVD Polycrystalline SiGe and Ge

2.3.5.1 Material Properties and Process Generalities

Germanium (Ge) and silicon–germanium (SiGe) are of interest to the MEMS community because of the low temperatures required to deposit polycrystalline films, making them potentially compatible with Si CMOS structures in integrated MEMS devices. Polycrystalline Ge (poly-Ge) films can be deposited by LPCVD at temperatures as low as 325°C on Si, Ge, and silicon–germanium (SiGe) substrate materials [88]. Ge does not readily nucleate on SiO_2 surfaces, which hinders the use of thermal oxides and LTO films as sacrificial layers, but facilitates the use of patterned oxide films as sacrificial molds. Residual stress in poly-Ge films deposited

on Si substrates can be reduced to nearly zero after anneals at modest temperatures (∼600°C). Poly-Ge is essentially impervious to KOH, TMAH, and BOE, enabling the fabrication of Ge structures on Si substrates by anisotropic etching [88]. The mechanical properties of poly-Ge are comparable with polysilicon, with a Young's modulus of 132 GPa and a fracture stress ranging between 1.5 and 3.0 GPa [89]. Mixtures of HNO_3, H_2O, and HCl and H_2O, H_2O_2, and HCl can be used to isotropically etch Ge, enabling poly-Ge to be used as a sacrificial substrate layer in polysilicon surface micromachining. Using these techniques, poly-Ge-based thermistors and Si_3N_4 membrane-based pressure sensors made using poly-Ge sacrificial layers have been successfully fabricated [88]. Poly-Ge deposition processes are temperature-compatible with Si CMOS as shown by Franke et al. who found no performance degradation in Si CMOS devices following the fabrication of surface micromachined poly-Ge structures [89].

Like poly-Ge, polycrystalline SiGe (poly-SiGe) is a material that can be deposited at temperatures lower than polysilicon. Although the name implies a Si-to-Ge ratio of 1:1, the ratio of Si to Ge in the films does not have to be unity. Deposition processes use SiH_4 and GeH_4 as precursor gases. Deposition temperatures range between 450°C for conventional LPCVD [90] and 625°C for rapid thermal CVD (RTCVD) [91]. Like polysilicon, poly-SiGe can be doped with boron and phosphorus to modify its conductivity. In situ boron doping can be performed at temperatures as low as 450°C [90]. Sedky et al. [92] showed that the deposition temperature of conductive films doped with boron could be further reduced to 400°C if the Ge content was kept at or above 70%. Films grown at temperatures around 400°C exhibit a strain gradient in the range of $\sim 1 \times 10^{-5}/\mu m$, which has been attributed to the columnar microstructure of the films combined with a high compressive stress at the film/substrate interface [93]. Boron doping enhances uniformity in the columnar microstructure through the thickness of the film and thus reduces the strain gradient. It has recently been reported that deposition temperatures for poly-SiGe can be reduced to 210°C, however, to achieve strain gradients on the order of $1 \times 10^{-6}/\mu m$, the films must be annealed following deposition [94].

Unlike poly-Ge, poly-SiGe can be deposited on SiO_2 [91], PSG [89] and poly-Ge [89] substrates. For growth of Ge-rich films on oxide substrate layers, a thin polysilicon seed layer is sometimes used to enhance nucleation. As with many alloys, the physical properties of the material depend on chemical composition. For example, etching of poly-SiGe by H_2O_2, becomes significant for Ge concentrations over 70%. Sedky et al. [92] showed that the microstructure, film conductivity, residual stress, and residual stress gradient are related to the concentration of Ge in the material. Franke et al. [90] produced in situ boron-doped films with residual compressive stresses as low as 10 MPa.

The poly-SiGe/poly-Ge material system is particularly attractive for surface micromachining inasmuch as H_2O_2 can be used to dissolve poly-Ge sacrificial layers. It has been reported that poly-Ge etches at a rate of 0.4 μm/min in H_2O_2, whereas poly-SiGe with Ge concentrations below 80% have no observable etch rate after 40 h [95]. The ability to use of H_2O_2 as a sacrificial etchant makes the combination of poly-SiGe and poly-Ge attractive for surface micromachining

from processing, safety, and materials compatibility points of view especially when compared with the polysilicon/silicon dioxide material system. Poly-SiGe structural elements, such as gimbal-based microactuator structures have been made by high-aspect-ratio micromolding [95]. PolySiGe has a lower thermal conductivity than Si, making it a well-suited alternative to polysilicon for thermopiles [96].

Poly-SiGe films exhibit a residual stress that can either be moderately tensile or moderately compressive depending on the Ge content and deposition temperature [92, 97]. For instance, it was found that for polySiGe films deposited by LPCVD at 450°C, the residual stress ranged from –31 MPa for a film with a Ge concentration of 64 at % to –160 for a Ge concentration of 47 at.% [97]. Annealing can be used to reduce both stress and stress gradients, and in fact, RF MEMS structures fabricated from poly-SiGe have shown a nearly twofold increase in quality factor if the films are annealed at 600°C [98]. Unfortunately the temperature-sensitive substrates on which the poly-SiGe films are usually deposited ultimately limits the extent to which annealing can be performed. It has been shown that pulsed laser annealing can be an effective means to locally eliminate stress gradients in poly-SiGe films [99].

As mentioned previously, poly-SiGe is well suited as a structural layer for integrated MEMS [90]. The low deposition temperatures associated with poly-SiGe structural components and polyGe sacrificial layers enable the fabrication of complete Si CMOS structures prior to MEMS fabrication. Use of H_2O_2 as the sacrificial etchant eliminates the need for layers to protect the underlying CMOS structure during release. A significant advantage of this design lies in the fact that the MEMS structure can be positioned directly above the CMOS structure, thus reducing the parasitic capacitance and contact resistance characteristic of interconnects associated with conventional side-by-side integration strategies. Recent efforts to advance the use of poly-SiGe as a structural layer in CMOS integrated MEMS includes process development in a large-scale LPCVD furnace of a design-of-experiments methodology designed to explore the interplay among process parameters and thickness, residual stress, strain gradient, and resistivity [93] as well as strategies to realize low-resistance electrical contacts between poly-SiGe structures and interconnect metallization [100].

2.3.5.2 Process Selection Guidelines

Tables 2.28, 2.29, 2.30, and 2.31 provide process-related material property data for as-deposited and annealed SiGe films deposited by LPCVD.

2.3.6 LPCVD Polycrystalline Silicon Carbide

2.3.6.1 Material Properties and Process Generalities

Unlike Si, crystalline silicon carbide (SiC) is a polymorphic material that exists in cubic, hexagonal, and rhombohedral polytypes. Well over 100 possible polytypic configurations have been identified, but only three are technologically relevant

Table 2.28 Deposition conditions for LPCVD SiGe films on oxide coated Si substrates

References	Temp (°C)	Gas	Gas flow (sccm)	Pressure (torr)	Dep. rate (nm/min)	Thickness (μm)
[101]	450	Si_2H_6	15	0.3	7	
		GeH_4	185			
		PH_3 (50% in SiH_4)	5			
[101]	450	Si_2H_6	25	0.3	20	
		GeH_4	175			
		B_2H_6 (10% in SiH_4)	4			
[102]	400	GeH_4	219	0.3	21	5.1
		PH_3 (50% in SiH_4)	5			
	450	GeH_4	90	0.6	17	3.1
		SiH_4 (90% in B_2H_6)	50			
		SiH_4	85			
[103]	410–440	SiH_4	104–120	600	4.7–12.5	1.7–2.6
		GeH_4	50–70			
		BCl_3 (in He)	6–18			
[103]	350	GeH_4	100			
		BCl_3 (in He)	12	300	7.7	2.2

because methods exist to produce single crystalline substrates and/or epitaxial thin films. Two of these are hexagonal polytypes, denoted 4H-SiC and 6H-SiC, a nomenclature that references that stacking sequence of Si and C atoms. Both of these polytypes are available as single-crystalline wafers, and epitaxial films of the same polytype can be grown on these substrates. Owing to the challenges associated with micromachining SiC, the 4H- and 6H-SiC polytypes have seen limited use as structural elements in MEMS, although pressure transducers and accelerometers have been fabricated using selective photoelectrochemical etching [104] and deep reactive ion etching [105]. 4H- and 6H-SiC are both attractive for high-temperature electronics, due to their wide bandgaps, which are 2.9 and 3.2 eV for 6H-SiC and 4H-SiC, respectively. All polytypes of SiC do not melt, but rather sublime at temperatures in excess of 2200°C.

The third technologically relevant polytype is a cubic polytype known as 3C-SiC, which in fact is the only cubic configuration known to exist in SiC. Unlike its hexagonal counterparts, 3C-SiC is not commercially available as single-crystalline substrates, although several efforts over the years have been devoted to producing large-area single-crystalline wafers. 3C-SiC has a diamond lattice structure like Si that enables epitaxial growth of 3C-SiC films on Si wafers. This fact, coupled with the material properties of 3C-SiC makes it an attractive complement to Si for harsh environment MEMS [106]. The electronic bandgap of 3C-SiC is 2.3 eV, which is less than 6H-SiC but more than double that of Si (1.1 eV). 3C-SiC has a thermal conductivity of 5 W/cm °C, a breakdown field of 4×10^6V/cm, a dielectric constant

Table 2.29 Mechanical properties of silicon germanium films deposited by LPCVD

References	Temp (°C)	Gas	Gas flow (sccm)	Pressure (torr)	Thickness (μm)	Young's modulus (GPa)	Residual stress (MPa)	Fract. strain (%)	Strain gradient (10^4/μm)
[102]	400	GeH_4	219	0.3	5.1	132	–100	1.1	1.3
		SiH_4 (50% in PH_3)	5						
[102]	450	GeH_4	90	0.6	3.1	146	–10	1.2	1.9
		B_2H_6 (10% in SiH_4)	50						
		SiH_4	85						
[103]	410–440	SiH_4	104–120	0.6	1.7–2.6		–70 to –228		1.2–8.7
		GeH_4	50–70						
		BCl_3 (in He)	6–18						
[103]	350	GeH_4	100	0.3	2.2		–83		
		BCl_3 (in He)	12						
[101]	550	Si_2H_6	15	0.3	2		–50		
		GeH_4	185						
		PH_3 (50% in SiH_4)	5						

Table 2.30 Electrical properties of silicon germanium films deposited by LPCVD

References	Temp (°C)	Gas	Gas flow (sccm)	Pressure (torr)	Thickness (μm)	Resistivity (mΩ cm)
[102]	400	GeH_4	219	0.3	5.1	20
		PH_3 (50% in SiH_4)	5			
	450	GeH_4	90	0.6	3.1	1.8
		SiH_4 (90% in B_2H_6)	50			
[103]	410–440	SiH_4	104–120	0.6	1.7–2.6	0.96–10
		GeH_4	50–70			
		BCl_3 (in He)	6–18			
[103]	350	GeH_4	100			
		BCl_3 (in He)	12	0.3	2.2	5.0
[101]	550	Si_2H_6	15	0.3	2	20
		GeH_4	185			
		PH_3 (50% in SiH_4)	5			

Table 2.31 Mechanical properties of annealed silicon germanium films deposited by LPCVD[a]

Reference	Temp (°C)	Gas	Gas flow (sccm)	Pressure (torr)	Thickness (μm)	Residual stress (MPa)	Strain gradient (10^4/μm)
[102]	400	GeH_4	219	0.3	5.1	200	0.94
		PH_3 (50% in SiH_4)	5				

[a]Films annealed by rapid thermal annealing at 550°C for 30 s.

of 9.72, a coefficient of thermal expansion of 4.2×10^{-6}/°C and an electron mobility of 1000 cm^2/Vs, which is the highest of the three polytypes. The Young's modulus of 3C-SiC is still the subject of research, but most reported values range from 350 to 450 GPa, depending on the microstructure and measurement technique.

From a processing perspective, the 4H-SiC and 6H-SiC polytypes are not compatible with Si substrates due to the high temperatures required for film growth (>1500°C) as well as the incompatible crystalline structure (although one could argue that (111) Si presents a crystalline face that closely resembles a hexagonal configuration). In contrast, 3C-SiC can be grown directly on Si using the epitaxial processes described in more detail in Section 3.4.2 .

To first order, micromachining of SiC is independent of crystalline polytype. SiC is not etched in any wet Si etchants and is not attacked by XeF_2, a popular dry Si etchant used for releasing device structures [107]. Patterning of SiC films is performed by conventional reactive ion etching using fluorinated plasmas often mixed with O_2 and sometimes an inert gas. Selectivity to Si-based materials is a major issue and patterning with photoresist is not presently possible, at least for films in

the micron thickness range. Alternatives to photoresist for RIE masks include metals such as Al and Ni. Recent efforts in developing a RIE process for SiC surface micromachining have been successful in achieving an acceptable selectivity to SiO_2 [108].

Polycrystalline SiC (poly-SiC) is a more versatile material for SiC MEMS than its single-crystal counterparts because poly-SiC is not constrained to single-crystalline substrates but can be deposited on a variety of materials, including polysilicon, SiO_2, and Si_3N_4, Commonly used deposition techniques include LPCVD [107, 109, 110] and APCVD [111, 112]. The deposition of poly-SiC can be performed at temperatures ranging from 700 to 1200°C. The microstructure of poly-SiC films is dependent on the substrate material and the deposition process used to grow the films. For amorphous substrates such as SiO_2 and Si_3N_4, APCVD poly-SiC films deposited from SiH_4 and C_3H_8 are randomly oriented with equiaxed grains [112], whereas for oriented substrates such as polysilicon, the texture of the poly-SiC film can be made to match that of the substrate itself [111]. By comparison, poly-SiC films deposited by LPCVD from SiH_2Cl_2 and C_2H_2 are highly textured (111) films with a columnar microstructure [109], whereas films deposited from disilabutane have a distribution of orientations [107]. This variation suggests that device performance can be tailored by selecting the proper substrate and deposition conditions.

SiC films deposited by AP- and LPCVD generally suffer from large residual stresses that are tensile and on the order of several 100 MPa. Moreover, the residual stress gradients in these films tend to be large, leading to significant out-of-plane bending of structures anchored at a single location. The thermal stability of stoichiometric SiC makes a postdeposition annealing step impractical for films deposited on Si substrates, because the temperatures needed to significantly modify the film are likely to exceed the melting temperature of the wafer.

2.3.6.2 Process Selection Guidelines

Poly-SiC can be deposited by LPCVD using a wide range of carbon and silicon containing precursors; however, relatively recent efforts to develop the material specifically for MEMS applications have focused on two approaches: a dual precursor approach using acetylene and dichlorosilane [113, 116], and a single precursor approach based on disilabutane [114]. Both of these development efforts were performed using large-scale, horizontal furnaces so as to mimic the deposition processes used for polysilicon, silicon nitride, and LTO/PSG. Tables 2.32, 2.33, 2.34, and 2.35 summarize the principle findings of these groups as well as other notable efforts reported in the literature.

2.3.6.3 Case Studies

Widespread adoption of poly-SiC as a structural material for MEMS applications has been hindered by the large residual stresses (for the most part tensile) and associated stress gradients in films deposited on Si substrates. Unlike polysilicon, for

Table 2.32 Deposition conditions for dichlorosilane-based LPCVD poly-SiC processes[a]

References	Temp (°C)	Gas	Gas flow (sccm)	Pressure (torr)	Thickness (μm)	Dep. rate (nm/min)
[115]	800	DSB[b]	45			4.2–5.3
		DCS[c]	0–40			
[116]	900	DCS	54	2.5–5	∼0.5	3–5
		C_2H_2 (5% in H_2)	180			
[117]	900–1000	DCS	10	0.150	0.7–5	4.8
[118]		C_2H_2	10			

[a]Denoted biaxial modulus
[b]DSB: 1,3 Disilabutane (SiH_3-CH_2-SiH_2-CH_3)
[c]DCS: Dichlorosilane (SiH_2Cl_2)

which the residual stresses can be significantly altered by annealing, poly-SiC, for the most part, is immune to structural alteration, at least for annealing conditions compatible with Si substrates. Efforts have been made to address this issue for both the dual and single precursor approaches by developing methods to control residual stress during the deposition process. For the SiH_2Cl_2- and C_2H_2-based dual precursor system, a relationship between deposition pressure and residual stress has been found that enables the deposition of undoped poly-SiC films with nearly zero residual stresses and negligible stress gradients [113]. This work was performed in a MRL^{TM} Model 1118 LPCVD furnace modified to support poly-SiC growth at a temperature of 900°C (see Tables 2.31 and 2.33 for more details). The pressure range where the residual stress was observed to vary significantly was between ∼0.5 and 5 torr. In the lower range of pressures (<2.5 torr) the residual stress was tensile, decreasing from ∼700 MPa at 0.5 torr to ∼50 MPa at 2.5 torr. For pressures above 3 torr, the residual stress was moderately compressive at –100 MPa. The behavior was attributed to differences in alignment and size of the columnar <111> oriented grains in the films. A similar dependence on deposition pressure was also observed when NH_3 was used as an in situ doping precursor, although the minimum residual stress (29 MPa) was observed at a pressure of 5 torr and a transition to compressive stresses was not observed [128]. The minimum resistivity in these films was 0.017 Ω cm, and this occurred at a deposition pressure of 4 torr and a residual stress of ∼60 MPa.

Like the dual precursor approach, development of poly-SiC film processes using the single precursor DSB focused on identifying a process that produced low-stress, highly conductive films. Early work centered on producing high-conductivity films using NH_3 as the doping gas [134, 135]. Films were grown at temperatures ranging from 650 to 850°C [135]. A minimum conductivity of 0.02 Ω cm was reported for films deposited at a temperatures of 850°C when using NH_3 as a doping gas [134]. At a deposition temperature of 800°C, the resistivity of as-deposited films is roughly 0.028 Ω cm, but this can be reduced to nominally 0.02 Ω cm when the film is annealed at 1000°C [135].

Table 2.33 Deposition conditions for non-dichlorosilane-based LPCVD poly-SiC processes

References	Temp (°C)	Gas	Gas flow (sccm or ratio)	Pressure (torr)	Thickness (μm)	Dep. rate (nm/min)
[119]	780	DSB[a]	na	5×10^{-5}	0.6	3.5
[120]	800	DSB	5	0.1	1	
		NH_3 (5% in H_2)	NH_3: DSB = 0.05			
[121]	800	DSB	5		2	
		NH_3 (10% in H_2)	2			
[120]	850	DSB	5	0.11	2	
		TMA[b]	TMA: DSB = 0.1			
[122]	930–1150	TMS[c]	10	0.4	0.33–1.35	
		H_2	1000			
[123]	1100	3MS	40	4–8	1–3	
		H_2	1000			
[124]	1010	SiH_4	15	2.48	1	
		C_2H_2	7			
		HCl	Trace			
		H_2	10,000			
		B_2H_6	1.5			
[125]	1100	SiH_4	1.5	40	2	
		C_2H_4	4.5			
		H_2	3000			
		NH_3	0–5			

[a]DSB: 1,3 Disilabutane (SiH_3-CH_2-SiH_2-CH_3)
[b]TMA: Trimethyl aluminum: ($Al(CH_3)_3$)
[c]TMS: Tetramethylsilane ($Si(CH_3)_4$)

Table 2.34 Mechanical properties of poly-SiC films deposited by LPCVD

References	Temp (°C)	Gas	Gas flow (sccm or ratio)	Pressure (torr)	Thickness (μm)	Young's modulus (GPa)	Tensile strength (GPa)	Residual stress (MPa)	Fracture toughness (MPa$\sqrt{m}$)
[121]	800	DSB[a]	5		2		23.4		
		NH_3 (10% in H_2)	2						
[115]	800	DSB	45						
		DCS[b]	0–40					240–1.2	
[116]	900	DCS	54	2.5–5	0.531			–98 to 172	
		C_2H_2 (5% in H_2)	180						
[126]	900	DCS	35	2	2.7	403		56	
		C_2H_2 (5% in H_2)	180						
[127]	900	DCS	54	2.75		373		26.9	
		C_2H_2 (5% in H_2)	180						
[128]	900	DCS	35	4		334		59	2.9–3.0
[129]		C_2H_2 (5% in H_2)	180						
		NH_3 (5% in H_2)	64						
[117]	900	DCS	10	0.150	0.7–5	347		30–250	
[118]	1000	C_2H_2	10						
[122]	930–1150	TMS[c]	10	0.4	0.33–1.35			–176 to 145	
		H_2	1000						

Table 2.34 (continued)

References	Temp (°C)	Gas	Gas flow (sccm or ratio)	Pressure (torr)	Thickness (μm)	Young's modulus (GPa)	Tensile strength (GPa)	Residual stress (MPa)	Fracture toughness (MPa$\sqrt{m}$)
[124]	1010	SiH_4	15	2.48	1	530		300	
		C_2H_2	7						
		HCl	Trace						
		H_2	10,000						
		B_2H_6	1.5						
[123]	1100	3MS	40	4–8	1–3			120	
		H_2	1000						
[130]	1200	3MS	35						
		H_2	1000					188	
		N_2	1						
[131]	1200	SiH_4	na	40	0.04–1.4	322–415*	3.2–6.5	192–347	
		C_2H_4	na						
[132]	1280	C_3H_8	C/Si: 0.8 –1	300		246			
		SiH_4							
		H_2 (2% Ar)	SiH_4/H_2: 0.024%						
		C_2H_2 (5% in H_2)	180						

[a]DSB: 1,3 Disilabutane (SiH_3-CH_2-SiH_2-CH_3)
[b]DCS: Dichlorosilane (SiH_2Cl_2)
[c]TMS: Tetramethylsilane ($Si(CH_3)_4$)
*Plane-strain modulus

Table 2.35 Electrical properties of poly-SiC films deposited by LPCVD

References	Temp (°C)	Gas	Gas flow (sccm or ratio)	Pressure (mtorr)	Thickness (μm)	Resistivity (Ω cm)
[120]	800	DSB[a]	5	100		1000
[120]	800	DSB	5	100	1	0.03
		NH_3 (5% in H_2)	5:100[b]			
[120]	850	DSB	5	110	2	16
		TMA[c]	10:100[d]			
[133]	900	DCS[e]	35	2000	1	
		C_2H_2 (5% in H_2)	180			
		NH_3 (1% in H_2)	20			1.466
		NH_3 (1% in H_2)	100			0.036
[128]	900	DCS	35	4000		0.017
		C_2H_2 (5% in H_2)	180			
		NH_3 (5% in H_2)	64			
[124]	1010	SiH_4	15	2.48	1	0.01
		C_2H_2	7			
		HCl	Trace			
		H_2	10000			
		B_2H_6	1.5			
[125]	1100	SiH_4	1.5	40	2	
		C_2H_4	4.5			
		H_2	3000			
		NH_3	0			0.56
		NH_3	5			1×10^{-3}
[130]	1200	3MS	35			
		H_2	1000			4×10^{-2}
		N_2	1			

[a]DSB: 1,3 Disilabutane (SiH_3-CH_2-SiH_2-CH_3)
[b]Ratio of NH_3 to DSB
[c]TMA: Trimethyl aluminum: ($Al(CH_3)_3$)
[d]Ratio of TMA to DSB
[e]DCS: Dichlorosilane (SiH_2Cl_2)

In order to modify residual stresses and stress gradients in DSB-based poly-SiC films, several approaches have been explored. One approach uses a method similar to the Multi-poly process described earlier in this chapter. For DSB-based, nitrogen-doped poly-SiC films exhibiting a resistivity of 0.02–0.03 Ω cm, the average strain is roughly 0.2% [136]. However, as the resistivity increases to ∼20 Ω cm in undoped films, the average strain drops to 0.1%. By properly sequencing doped and undoped poly-SiC layers, a 3 μm thick film with a strain gradient of $5 \times 10^{-5}/\mu m$ and a resistivity of 0.024 Ω cm could be produced [136].

A second approach to adjust residual stress in DSB-based poly-SiC films involves the use of a Si-containing precursor to adjust the chemical composition of the poly-SiC film [137]. In this method, DCS is used as the additional source of Si. Films were grown at 800°C using a DSB flow rate of 45 sccm, and the DCS flow rate was

varied to achieve DCS-to-total gas flow ratios from 0 to ∼0.5. Under these conditions, the Si-to-C ratio in the as-deposited films varied from 1 to ∼1.2. Likewise, residual stresses varied from 1.2 GPa for a Si-to-C ratio of 1 (no DCS flow) to 240 MPa for a Si-to-C ratio of 1.2. The mechanism responsible for the significant drop in residual stress is linked to an increase in grain size with increasing DCS flow, as well as a higher concentration of Si in the films.

A third approach to modify residual stress in DSB-based poly-SiC films involves a postdeposition anneal. It was recently shown that a postdeposition annealing step performed at temperatures between 925 and 1050°C on doped poly-SiC films deposited at 800°C using DSB and DCS precursors is effective at shifting the residual stress from nominally 400 MPa to roughly –300 MPa and reducing the resistivity from ∼0.07 to ∼0.03 Ω cm [138].

2.3.7 LPCVD Diamond

2.3.7.1 Material Properties and Process Generalities

Diamond has a collection of physical properties that makes it very attractive for a wide range of MEMS materials [106]. Diamond is commonly known as nature's hardest material, making it ideal for high wear environments. Diamond has a very large electronic bandgap (5.5 eV) which makes it attractive for high-temperature electronics. Undoped diamond is a high-quality insulator with a dielectric constant of 5.5; however, it can be relatively easily doped with boron to create p-type conductivity, and n-type conductivity can be achieved by doping with nitrogen. The electron mobility in diamond exceeds that of 3C-SiC at 2200 cm^2/Vs, and it has a breakdown field of 1×10^7 V/cm. Diamond has the highest Young's modulus among the materials used in MEMS (1035 GPa) and a thermal conductivity of 20 W/cm °C, which is double that of SiC and over ten times that of Si. Diamond is among nature's most chemically inert materials except perhaps in oxidizing atmospheres.

Diamond thin films used in MEMS are polycrystalline in microstructure and are often classified by the size of the crystallites in the film. Nucleation of diamond films on nondiamond substrates from the gas phase is challenging without the aid of a seed layer. Substrate seeding often involves sonication of the substrate with nano- or microscale diamond particles. An alternative called biased-enhanced nucleation (BEN) has eliminated the need for sonication and is particularly well suited when plasma techniques are used to grow the films. Micro- and nanocrystalline diamond films are typically grown by hot filament or microwave plasma CVD methods using a hydrocarbon precursor such as methane combined with hydrogen gas. The grain size is, in part, determined by the diameter and density of the seed particles. Atomic hydrogen is responsible for suppressing the growth of sp^2 bonded carbon. A relatively recent development in thin film diamond technology is ultrananocrystalline diamond (UNCD). UNCD films are particularly attractive for MEMS due to their outstanding physical and chemical properties and combined low deposition temperatures, making them more compatible with a wider range of MEMS materials than

their micro- and nanocrystalline counterparts. In terms of materials properties, it has been shown that UNCD films exhibit a measured hardness of 98 GPa, a Young's modulus of ~960 GPa and a fracture strength ranging from 3990 to 5080 MPa [139]. By comparison, similar test specimens made from single-crystalline 3C-SiC had a measured Young's modulus of ~435 GPa and a fracture strength of 2090–2680 MPa [139].

Fabrication of diamond MEMS is currently restricted to polycrystalline material inasmuch as single-crystal diamond wafers are not yet commercially available and thus epitaxial growth for MEMS is not feasible. Diamond films can be deposited on Si and SiO_2 substrates by CVD methods, but the surfaces must be seeded by diamond powders or biased with a negative charge to initiate growth. In general, microcrystalline diamond prefers to nucleate on Si surfaces than on SiO_2 surfaces, an effect that has been used to selectively pattern diamond films using SiO_2 molding masks [140].

2.3.7.2 Process Selection Guidelines

Tables 2.36, 2.37, and 2.38 provide process-related details for micro-, nano- and ultrananocrystalline diamond films used in MEMS fabrication.

2.3.7.3 Case Studies

Patterning of diamond structures is arguably the most challenging aspect of diamond MEMS fabrication due to the chemical inertness of the material. Early methods to pattern diamond included: use of Si molds to create bulk micromachined diamond structures [152], selective seeding using diamond-loaded photoresist [153], patterning seed layers using photoresist liftoff [154], O_2 ion beam etching of diamond thin-films [155], and biased enhanced nucleation through patterned SiO_2 masks [156]. Wang et al. [157] developed a process to fabricate a vertically actuated, doubly clamped micromechanical diamond beam resonator using conventional RIE. In this process diamond films grown by MPCVD on SiO_2 sacrificial layers were etched in a CF_4/O_2 plasma using Al as a hard mask. The etch was reasonably selective to SiO_2 (15:1), enabling the fabrication of diamond disk resonators suspended on a polysilicon stem with polysilicon drive and sense electrodes [158]. Along similar lines, Sepulveda et al. have successfully fabricated surface micromachined diamond cantilever-beam resonators by RIE using silicon dioxide as a sacrificial layer and a Ti film as an etch mask [159].

Microcrystalline diamond films grown using conventional techniques tend to have high residual stress gradients and roughened surfaces as a result of the highly faceted, large-grain polycrystalline films that are produced by these methods. The rough surface morphology degrades the patterning process, resulting in roughened sidewalls in etched structures and roughened surfaces of films deposited over these layers. Unlike polysilicon and SiC, a postdeposition polishing process is not technically feasible for diamond due to its extreme hardness. To address this issue, Krauss et al. [145] have developed an ultrananocrystalline diamond (UCND) film

Table 2.36 Deposition conditions and material properties of micro and nanocrystalline diamond deposited by MPCVD[a]

References	Temp (°C)	Gas	Gas flow (sccm)	Power (W)	Pressure (torr)	Young's modulus (GPa)	Tensile strength (GPa)	Residual stress (MPa)	Resistivity (Ω cm)
[141]	450–550	CH_4	3	700	6.75–15	741–913	0.7		
		CO_2	8						
		H_2	200						
	625–725	CH_4	3	700	20–33	710–1015	0.8–1.6		
		CO_2	8						
		H_2	200						
[142]	400–800	CH_4	6	800		450–1050		550 to –440	
		H_2	30						
		Ar	564						
[143]	800	CH_4	6	800	97.5			200–1200	
		H_2	12–60						
		Ar	582–532						
[144]	850	CH_4	5	1500	40				0.2–300
		H_2	500						

[a]Film thickness: 0.5–5 μm

Table 2.37 Deposition conditions and properties of ultrananocrystalline diamond (UNCD) by MPCVD

References	Temp (°C)	Gas	Gas flow (sccm)	Power (W)	Pressure (torr)	Thickness (μm)	Young's modulus (GPa)	Tensile strength (GPa)	Fracture toughness (MPa$\sqrt{m}$)
[145]	300–800	CH_4 Ar	1 99		100		700–1000		
[146]	na	na	na			0.5–0.6	941–963	3.9–5.0	
[147]	800	CH_4 Ar	na na		100	0.6–0.8	975	0.89–5.0	

Table 2.38 Deposition conditions and properties of polycrystalline diamond deposited by HFCVD[a]

References	Temp (°C)	Gas	Gas flow (sccm)	Pressure (torr)	Young's modulus (GPa)	Tensile strength (GPa)	Residual stress (MPa)	Resistivity (Ω cm)
[148]	680–740	CH_4 (0.3% in H_2)	400	11.25	600–1010	2.8–3.25	<5	
[149]	680	CH_4 H_2	na na		790		–370	0.2–300
[150]	800–900	CH_4 H_2	4 400	50				0.29–116
[151]	900	CH_4 (1% in H_2)		50				0.03–0.28

[a]Film thickness: 1–20 μm

that exhibits a much smoother surface morphology than its micro- and nanocrystalline counterparts. Unlike conventional CVD diamond films that are grown using a mixture of H_2 and CH_4, the ultrananocrystalline diamond films are grown from mixtures of Ar, H_2, and C_{60} or Ar, H_2, and CH_4. A typical process uses a 2.56 GHz MPCVD system with a precursor mixture consisting of 1% CH_4 balanced with Ar at a flow rate of 100 sccm and substrate temperatures in the 350–800°C range [160].

The process is in stark contrast with conventional HF- or MPCVD growth of diamond where a high concentration of hydrogen is used to suppress formation of sp^2 bonded carbon. The absence of hydrogen ensures that a very high density of ultrasmall nuclei ($\sim 10^{11}/cm^2$) form on the substrate surface. A typical film grown at 400°C consists of 3–5 nm equiaxed grains grown at rates as high as 0.4 μm/h [160]. UNCD films have proven to be effective as conformal coatings on Si surfaces, and have been used successfully in several surface micromachining processes [160]. Unlike diamond films grown by conventional means, the CH_4–Ar precursor system used in UNCD growth enables direct nucleation on SiO_2 surfaces, thus making UNCD highly compatible with conventional surface micromachining. For patterning, an oxygen-resistant hard mask such as SiO_2 is used in conjunction with a oxygen plasma. UNCD is highly resistant to HF, thus enabling the release of suspended structures. UNCD can readily be doped with nitrogen resulting in n-type conductivity with semimetal-like behavior in heavily doped samples.

Given the large bandgap of diamond (5.5 eV), UNCD is proving to be among the most versatile materials in the MEMS materials toolbox because films with

electrical properties ranging from highly insulating to highly conductive can be produced by controlled incorporation of dopants. At substrate temperatures of 400°C, the UNCD growth process is highly compatible with Si CMOS integration [161]. UNCD films tend to have lower stresses and stress gradients than micro- and nanocrystalline diamond films [148]. The hydrogen-terminated surfaces of ultrathin (submicron) UNCD films functionalized with DNA oligonucleotides exhibit a high degree of chemical stability and sensitivity, making them particularly well suited for biosensor applications [162].

2.3.8 APCVD Polycrystalline Silicon Carbide

2.3.8.1 Material Properties and Process Generalities

Like LPCVD, APCVD can be used to deposit poly-SiC films. The APCVD process is much less common than its LPCVD counterpart, but historically it was one of the first techniques used to deposit poly-SiC for MEMS applications and still remains a viable method. Like LPCVD poly-SiC, the properties of APCVD poly-SiC depend on the substrate temperature and material of the substrate. The most commonly used precursors are propane (C_3H_8) and SiH_4, with ultrahigh purity H_2 used as a carrier gas. However, any precursor or combination of precursors that contain Si and C are potential candidates. The deposition temperatures of APCVD poly-SiC tend to be several hundred degrees Celsius higher than LPCVD.

2.3.8.2 Process Selection Guidelines

Table 2.39 details relevant process information and mechanical property data for poly-SiC films deposited by APCVD.

2.3.9 PECVD Silicon

2.3.9.1 Material Properties and Process Generalities

Although much less commonly used than its LPCVD counterpart, PECVD has emerged as an alternative to LPCVD for the production of Si-based surface micromachined structures on temperature-sensitive substrates due to the much lower deposition temperatures needed to deposit the films. Gaspar et al. [166] reported on the development of surface micromachined microresonators fabricated from hydrogenated amorphous Si (a-Si:H) thin films deposited by PECVD. The vertically actuated resonators consisted of doubly clamped microbridges suspended over fixed Al electrodes. The a-Si:H films were deposited using SiH_4 and H_2 precursors and PH_3 as a doping gas. The substrate temperature was held to around 100°C, which enabled the use of photoresist as a sacrificial layer. The microbridges consisted of a large paddle suspended by two thin paddle supports, with the paddle providing a

Table 2.39 Deposition conditions and film properties for poly-SiC films deposited by APCVD

References	Substrate	Temp (°C)	Gas	Gas flow (sccm)	Thickness (μm)	Young's modulus (GPa)	Residual stress (MPa)	Fracture toughness (MPa$\sqrt{m}$)
[163]	SiO_2	1050	SiH_4 (5% in H_2) C_3H_8 (15% in H_2) H_2	204 52 25,000	2.8		150–214	2.8–3.4
[164]	Si	1100	HMDS[a] (90% in H_2)	na		367		
[165]	Poly	1160	SiH_4 (5% in H_2) C_3H_8 (15% in H_2) H_2	26 102 25,000	2	494	113	
[165]	Poly	1280	SiH_4 (5% in H_2) C_3H_8 (15% in H_2) H_2	26 102 25,000		340–357	401–486	

[a]HMDS: Hexamethyldisilane: $((CH_3)_6Si_2)$

large reflective surface for optical detection of resonant frequency. The megahertz-frequency resonators exhibited quality factors in the 1×10^5 range when tested in vacuum. This work has since been extended to using polynorbornene polymer as a sacrificial layer material [167]. A polynorbornene known as Unity 4011™ thermally decomposes into vapor at 425°C, enabling a dry, nonplasma-based release process. Surface micromachined resonators were successfully fabricated from a-Si:H films deposited by PECVD using this method. Cracking observed near the anchor points of some structures was attributed to differences in thermal expansion coefficients.

Chang and Sivoththaman have used conventional photoresist as a sacrificial layer to fabricate a tunable RF MEMS inductor based on PECVD Si [168]. In this case, photoresist could be used because the PECVD Si film was deposited at a temperature of only 150°C. The as-deposited films exhibited a residual compressive stress of about 300 MPa. The PECVD Si films were used in conjunction with sputtered Al with a residual tensile stress of nominally 10 MPa to create bimorph inductors whose stress-induced vertical displacement could be regulated by an actuation voltage.

2.3.9.2 Process Selection Guidelines

Tables 2.40, 2.41, and 2.42 provide process-related details and material property data for as-deposited and annealed SiC films deposited by PECVD.

2.3.10 PECVD Silicon Dioxide

2.3.10.1 Material Properties and Process Generalities

PECVD is perhaps the most common method to produce silicon dioxide films. Using a plasma to dissociate the gaseous precursors, the deposition temperatures needed to deposit PECVD oxide films are lower than for LPCVD films by as much as several hundred degrees. Commonly used source gases include single precursors such as TEOS or dual precursors such as SiH_4 and N_2O. PECVD oxides are commonly used as masking, passivation, and protective layers especially on devices that have been coated with metals. For this reason, residual stress is the principle property of interest for process engineers considering PECVD SiO_2 films in MEMS structures. Residual stress is heavily dependent on process parameters which in turn may be dictated by the substrate. Annealing has been shown to be an effective means to modify residual stress in PECVD oxide films, both to reduce the magnitude of stress as well as to change its state.

2.3.10.2 Process Selection Guidelines

Tables 2.43 and 2.44 summarize the process-related material property data for SiO_2 films deposited by PECVD.

Table 2.40 Deposition parameters and insulating properties for Si films deposited by PECVD

References	Temp (°C)	Gas	Gas flow (sccm or ratio)	Power or power density	Pressure (torr)	Dep. rate (nm/min)	Thickness (μm)	Conductivity (1/Ω cm)
[169]	150	SiH_4	10	77–114 mW/cm^2	0.5–0.75	22–31	0.5–3	Dark: 10^{-10}
		Ar	7					Light: 10^{-6}
[170]	250	SiH_4/H_2	10	50 mW/cm^2	0.1	0.6–2.4	0.1–0.8	10^{-3}
[171]		PH_3	na					
[172]	300	SiH_4	1/4–1/8	100–300 W	0.8	75		
		Ar						
[173]	300	SiH_4	40	50–215 W	0.38–0.53	7–16	1	
		Ar	20					

Table 2.41 Mechanical properties of Si films deposited by PECVD

References	Temp (°C)	Gas	Gas flow (sccm or ratio)	Power or power density	Pressure (torr)	Thickness (μm)	Young's modulus (GPa)	Residual stress (MPa)
[169]	150	SiH_4	10	77–114 mW/cm^2	0.5–0.75	0.5–3		–370
		Ar	7					–130
[170]	250	SiH_4/H_2	10	50 mW/cm^2	0.1	0.1–0.8	146	
[171]		PH_3	na					
[172]	300	SiH_4	1/4–1/8	100–300 W	0.8			–360 to –380
		Ar						
[173]	300	SiH_4	40	50–215 W	0.38–0.53	1		–520 to –575
		Ar	20					

Table 2.42 Mechanical properties of annealed Si films deposited by PECVD[a]

Reference	Temp (°C)	Gas	Gas flow (sccm)	Power (W)	Pressure (torr)	Thickness (μm)	As-deposited residual stress (MPa)	Postanneal residual stress (MPa)
[173]	300	SiH_4 Ar	40 20	50–215	0.38–0.53	1	–520 to –575	300

[a]Annealing conditions: 100 min at 367°C

Table 2.43 Deposition conditions and mechanical properties of SiO_2 films deposited by PECVD

References	Temp (°C)	Gas	Gas flow (sccm)	Power (W)	Pressure (torr)	Dep. rate (μm/min)	Thickness (μm)	Residual stress (MPa)
[174]	60	SiH_4 [a] N_2O	430 710	HF: 20 LF: 20	1			–25
[174]	300	SiH_4 N_2O	430 710	HF: 20 LF: 20	1			–200
[5]	300	SiH_4 N_2O N_2	na na na					–397
[175]	350	TEOS O_2	2.3[b] 9500			0.25	3.2 12.5	∼–90 ∼–45
[175]	400	SiH_4 N_2O N_2	300 9500 1500			1	20	∼–80

[a]2% in N_2
[b]For TEOS, the flow rate is in ml/min. TEOS: tetraethylorthosilicate: $(Si(OC_2H_5)_4)$

Table 2.44 Mechanical properties of annealed SiO_2 films deposited by PECVD

References	Temp (°C)	Gas	Gas flow (sccm)	Thickness (μm)	As-deposited residual stress (MPa)	Annealing conditions	Residual stress after anneal (MPa)
[5]	300	SiH_4 N_2O N_2	na na na	0.3	–397	O_2, 800°C, 30 min	–172
[175]	350	TEOS O_2	2.3[a] 9500	3.2 12.5	∼–90 ∼–45	500°C 500°C	∼–80 <10
[175]	400	SiH_4 N_2O N_2	300 9500 1500	20	∼–80	500°C	20

[a]For TEOS, the flow rate is in ml/min. TEOS: tetraethylorthosilicate: $(Si(OC_2H_5)_4)$

2.3.11 PECVD Silicon Nitride

2.3.11.1 Material Properties and Process Generalities

PECVD silicon nitride (sometimes referred to simply as SiN or Si_xN_y:H) is generally nonstoichiometric and may contain significant concentrations of hydrogen. Use of PECVD silicon nitride in micromachining applications is somewhat limited because it has a high etch rate in HF (e.g., often higher than that of thermally grown SiO_2). However, PECVD offers the ability to deposit nearly stress-free silicon nitride films at temperatures lower than LPCVD-based low-stress nitride, an attractive property for passivation, encapsulation, and packaging. Like its Si and SiO_2 counterparts, PECVD SiN is commonly deposited using SiH_4 as the silicon-containing precursor gas with NH_3 being the nitrogen-containing precursor. Deposition temperatures are considerably lower than for LPCVD silicon nitride, ranging from roughly 100 to 300°C. Load deflection measurements using bulk micromachined square and rectangular membranes have shown that Si_xN_y:H thin-films (∼300–700 nm) deposited by PECVD have a Young's modulus that increases with increasing deposition temperature, from 79 GPa at 125°C to 151 at 205°C [176]. The residual stresses in these films are below 30 MPa for each deposition temperature.

Table 2.45 Deposition parameters for silicon nitride films deposited by PECVD

References	Sub	Temp (°C)	Gas	Gas flow (sccm)	Power (W)	Pressure (torr)	Dep. rate (μm/min)	Thickness (μm)
[177]	Si	300	SiH_4	24	100	0.5–2	0.5–2.6	∼0.5
			NH_3	72–96				
[178]	Si	300	SiH_4	120	600	0.85	0.25–0.32	1
			NH_3	75				
			N_2	1200				

2.3.11.2 Process Selection Guidelines

Tables 2.45, 2.46, 2.47, 2.48, and 2.49 summarize the processing recipes and associated mechanical property data for silicon nitride films deposited by PECVD.

2.3.12 PECVD Silicon Germanium

2.3.12.1 Material Properties and Process Generalities

PECVD offers the same advantages to SiGe as it does to Si, SiO_2, and Si_3N_4, namely the ability to deposit the material at much lower deposition temperatures. SiGe is polycrystalline when deposited by PECVD at temperatures as low as 350°C, making

Table 2.46 Mechanical properties of silicon nitride films deposited by PECVD

References	Temp (°C)	Gas	Gas flow (sccm)	Power (W)	Pressure (torr)	Thickness (μm)	Young's modulus (GPa)	Residual stress (MPa)
[179]	50–300	SiH_4	5	100	0.45	0.5	50–150	–225 to 300
		NH_3	45					
		N_2	100					
[179]	55–330	SiH_4	5	75	0.88	0.7	150	–75 to 375
		NH_3	45					
		N_2	100					
[174]	60	SiH_4 *	1500	HF: 20	0.65			–121 to 36
		NH_3	5	LF: 20				
[180]	125–300	SiH_4		40–200	0.2–0.6	0.6–1.2	106–198	–250 to 250
		NH_3	10					
		N_2	2020					
[174]	300	SiH_4 *	1000	HF: 20	0.65			–850 to 300
		NH_3	20	LF: 20				
[181]	300	SiH_4	9	HF: 5	0.6		152	98
		NH_3	40	LF: 8				
		He	50					
[182]	300	SiH_4	600	100	0.9	0.68	133[a]	178
		N_2	1960					
		NH_3	55					
	300	SiH_4	600	100	0.9	0.68	140[a]	194
		N_2	1960					
		NH_3	55					
[83]	300	SiH_4	01:04.5		12	0.75		706
		NH_3						
[178]	300	SiH_4	120	600	0.85	1		4
		NH_3	75					
		N_2	1200					
[39]	300	SiH_4	15		0.5	0.5	210	110
		N_2	535					
[183]	350	SiH_4	2.4			0.5	112	
		N_2	1500					

*2% in N_2

[a]Plane-strain modulus

it attractive as an alternative structural material to polysilicon for electrostatically actuated MEMS. For SiGe MEMS, PECVD does offer one potential advantage over LPCVD when depositing films at such low temperatures, namely a higher growth rate, which is important for applications requiring film thicknesses in excess of 5 μm. The possible tradeoff for achieving higher growth rates is the increased likelihood that the films will have an amorphous microstructure and contain significantly more hydrogen than their microcrystalline LPCVD counterparts. The vast majority

Table 2.47 Fracture and failure data for silicon nitride films deposited by PECVD

Reference	Temp (°C)	Gas	Gas flow (sccm)	Power (W)	Pressure (torr)	Thickness (μm)	Biaxial modulus (GPa)	Residual stress (MPa)	Fracture strength (GPa)
[182]	300	SiH_4	600	100	0.9	0.68	133	178	1.53
		N_2	1960						
		NH_3	55						
	300	SiH_4	600	100	0.9	0.720	140	194	3.08
		N_2	1960						
		NH_3	55						

Table 2.48 Mechanical strain data for silicon nitride films deposited by PECVD

References	Temp (°C)	Gas	Gas flow (sccm)	Power (W)	Pressure (torr)	Thickness (μm)	Young's modulus (GPa)	Strain (10^{-3})	Ultimate strain
[177]	300	SiH_4	24	100	0.5–2	~0.5		–1.59 to 0.38	0.0022
		NH_3	72–96						
[183]	350	SiH_4	2.4			0.5	112	–0.626	
		N_2	1500						

Table 2.49 Hardness data for silicon nitride films deposited by PECVD [180]

Temp (°C)	Gas	Gas flow (sccm)	Power (W)	Pressure (mtorr)	Thickness (μm)	Young's modulus (GPa)	Residual stress (MPa)	Hardness (GPa)
125 to 300	SiH_4	1	40–200	2–6	0.58–1.2	106–198	–250 to 250	11.9–22.1
	NH_3	10						
	N_2	2020						

of PECVD processes use SiH_4 and GeH_4 as Si- and C-containing precursors. Like polysilicon, B_2H_6 and PH_3 are common p-type and n-type dopants.

2.3.12.2 Process Selection Guidelines

Tables 2.50, 2.51, 2.52, and 2.53 provide process information and material property data for as-deposited and annealed SiGe films deposited by PECVD.

2.3.12.3 Case Studies

Development of PECVD as an alternative to LPCVD for the production of SiGe films is motivated by the desire to have a process that has reasonably high growth rates at substrate temperatures that are compatible with CMOS processing. LPCVD

Table 2.50 Deposition parameters for silicon germanium films deposited by PECVD

References	Temp (°C)	Gas	Gas flow (sccm)	Power density (mW/cm^2)	Pressure (torr)	Dep. rate (nm/min)	Thickness (μm)
[184]	350	SiH_4	0–22	370	1	23 (Ge: 56%)	2
		GeH_4	0–22			21 (Ge: 42%)	
		H_2	2000				
		B_2H_6 (1% in H_2)	10				
[184]	400	SiH_4	0–22			23 (Ge: 67%)	
		GeH_4	0–22			20 (Ge: 48%)	
		H_2	2000				
		B_2H_6 (1% in H_2)	10				
[185]	520–610	SiH_4	42		0.45	48	2–4
		GeH_4	3				

Table 2.51 Mechanical and electrical properties of hydrogenated microcrystalline silicon germanium films deposited by PECVD [186][a]

Temp (°C)	Gas	Gas flow ratio	Power (W)	Dep. rate (nm/min)	Thickness (μm)	Residual stress (MPa)	Resistivity (mΩ cm)
	$H_2/(SiH_4 + GeH_4)$	91					
	$(SiH_4 + GeH_4)/B_2H_6$	233					
300	SiH_4/GeH_4	1.8	203	17	2	–175	75
350	SiH_4/GeH_4	1.8	203	16	1.9	2	18
400	SiH_4/GeH_4	1.5	203	17	2	–9	7
400	SiH_4/GeH_4	1.8	370	23	2	–25	9

[a]Deposition conditions: 1 torr on SiO_2/Si substrates

is typically characterized by low growth rates (~2–30 nm/min for LPCVD SiGe [187]), although the low growth rates are compensated by the large-scale furnaces that can accommodate >50 wafers per run. Nevertheless, growth of film thicknesses beyond 5 μm is not convenient in such systems, especially if low wafer volumes are required. PECVD, on the other hand, can produce films at much higher growth rates, and if substrate heating is used, the as-deposited films can be polycrystalline. Rusu et al. developed a PECVD process for poly-SiC that produces low-stress, high-conductivity polycrystalline films at deposition temperatures <600°C [187]. Specific process details are given in Table 2.51. They found that poly-SiGe films can be deposited directly onto SiO_2 substrate layers without the need of a nucleation

Table 2.52 Mechanical properties of doped silicon germanium films deposited by PECVD[a]

References	Temp (°C)	Gas	Gas flow (sccm)	Power (W)	Pressure (torr)	Dep. rate (nm/min)	Residual stress (MPa)	Strain gradient (10^4/μm)
[184]	350	SiH_4	0–22	370[b]	1	23 (Ge: 56%)	48	13.9
		GeH_4	0–22			21 (Ge: 42%)	–238	14
		H_2	2000					
		B_2H_6 (1% in H_2)	10					
[184]	400	SiH_4	0–22	370		23 (Ge: 67%)	25	3
		GeH_4	0–22			20 (Ge: 48%)	–32	6.3
		H_2	2000					
		B_2H_6 (1% in H_2)	10					
[185]	520–610	SiH_4	42		0.45	48	–18 to –225	
		GeH_4	3					
[187]	590	GeH_4	166	30	0.2		79	
		SiH_4	30					
		PH_3 (1% in SiH_4)	80					
[187]	520	GeH_4	166	30	0.2		19	
		SiH_4	30					
		PH_3 (1% in SiH_4)	40					
[187]	590	GeH_4	166	30	0.2		100	
		SiH_4	30					
		B_2H_6 (1% in H_2)	40					

[a]Film thickness range: 2–4 μm
[b]Power density in mW/cm^2

Table 2.53 Mechanical properties of annealed silicon germanium films deposited by PECVD[a]

Reference	Temp (°C)	Gas	Gas flow (sccm)	Pressure (torr)	Thickness (μm)	As-deposited residual stress (MPa)	Postanneal residual stress (MPa)
[185]	520–610	SiH_4 GeH_4	42 3	0.45	1	–18 to –225	200

[a]Film thickness: 2–4 μm

layer, and that the resulting films have moderate to low tensile stresses (<80 MPa). Films doped with PH_3 exhibit a reasonable conductivity (25 mΩ cm) and those doped with boron an even higher conductivity (0.64 mΩ cm). Moreover, films in the 2–10 μm thickness range could easily be deposited using a conventional commercially available PECVD system because the deposition rate is on the order of 200 nm/min.

Extensive work has been performed to use PECVD to lower the deposition temperatures of poly-SiGe to below 500°C. Mehta et al. describe a high growth rate process for poly-SiGe at temperatures on SiO_2 substrates as low as 300°C [188]. The authors used a standard, cold wall parallel plate reactor that can be operated in PECVD or LPCVD mode. To facilitate growth, the authors developed a multilayered process consisting of a thin (∼94 nm) SiGe seed layer deposited by PECVD which serves to promote nucleation of a LPCVD layer which is deposited directly on the seed layer and serves as a crystallization layer for bulk film growth by PECVD at temperatures that would otherwise lead to amorphous films. At 450°C, they were able to deposit a 1 μm thick $Si_{0.35}Ge_{0.65}$ film with an average residual stress of –5 MPa and a resistivity of 0.8–1.2 mΩ cm. The deposition rate at 450°C was 33 nm/min. For 11 μm-thick films produced under the same conditions, the average residual stress was 71 MPa, the average stress gradient was $3.6 \times 10^{-5}/\mu m$ and the resistivity was 0.9 mΩ cm. Films grown at 300°C under roughly the same gas flow and pressure conditions yielded a 2 μm thick film with a residual stress of –175 MPa and a resistivity of 75 mΩ cm. The growth rate was 17 nm/min. In a follow-up effort, this group explored means to reduce the stress gradient in these films and found that for 10 μm thick structures fabricated out of the aforementioned multilayered structure deposited at 450°C, a residual stress of 72 MPa and a stress gradient of 6.5 MPa/μm could be reduced to 57 MPa and 1.6 MPa/μm, respectively by the deposition of a 1.6 μm thick silicon-rich poly-SiGe film as the topmost layer of the structure [189]. Along similar lines, Mehta et al. showed that the seed layer need not be restricted to SiGe material [190]. They showed that a-Si can also be used not only to act as a nucleation surface, but also to provide a stress-compensating layer that reduces the thickness needed in the poly-SiGe capping layer. They were able to produce a 10 μm thick multilayered stack consisting of a thin a-Si seed layer and an 800 nm thick silicon-rich SiGe capping layer with an average stress of

35 MPa, a stress gradient of only $3.6 \times 10^{-6}/\mu m$ and a resistivity of 1.45 mΩ cm. The deposition rate was 90 nm/min.

For structures that suffer from excessive residual stresses and stress gradients in the as-fabricated state, annealing can be used to reduce their effects. However, the temperatures required for effective annealing may defeat the purpose of using the low-temperature deposition processes. To address this limitation, Sedky et al. have explored the use of KrF eximer laser processing for localized annealing of poly-SiGe structures [191]. In this work, films were deposited by PECVD at temperatures at and below 370°C, conditions that yield amorphous films. Laser parameters were selected to induce crystallization while avoiding conditions that would cause void formation due to excessive hydrogen out-diffusion as well as damage to structures beneath the SiGe films. The group found that subjecting a 0.77 μm thick amorphous $Si_{31}Ge_{69}$ film deposited at 300°C to 500 laser pulses at 70 mJ/cm^2 led to a reduction in residual stress from 93 to 48 MPa and the sheet resistance from 450 kΩ/sq to 0.6 Ω/sq. Moreover, a 0.4 μm thick $Si_{71}Ge_{29}$ film subjected to a single laser pulse at 500 mJ/cm^2 was effective at reducing the resistivity of the film from 12 kΩ cm to 1.3 mΩ cm.

2.3.13 PECVD Silicon Carbide

2.3.13.1 Material Properties and Process Generalities

SiC can be deposited at lower temperatures (25–400°C) by PECVD than either LPCVD or APCVD using many of the same precursors (both dual and single). For PECVD SiC films, the most commonly used precursors are SiH_4 and CH_4. The films are amorphous in microstructure and electrically insulating. As-deposited films typically have compressive residual stresses, but these can be converted to tensile stresses upon annealing at temperatures as low as 450°C. The films exhibit a much lower Young's modulus than their high temperature, polycrystalline counterparts, ostensibly due to hydrogen incorporation in the film as well as their amorphous microstructure. Hydrogen incorporation results from the fact that most precursors contain significant amounts of hydrogen. Annealing at 400°C can induce densification in hydrogenated films, and at temperatures above 800°C crystallization can occur. Like most PECVD films, the properties of SiC films deposited by PECVD are heavily dependent on process parameters, especially temperature inasmuch as it plays a key role in governing the amount of hydrogen that may get incorporated into the films.

PECVD SiC films are well suited for applications requiring a chemically resistant material. It has been reported elsewhere [192] that amorphous SiC films deposited by PECVD have an etch rate of <2 nm/h in KOH (33 wt% at 85°C), <2 nm/h in TMAH (25 wt% at 80°C), <1 nm/h in HF (40%) and 90–120 nm/h in HF/HNO_3 (2:5). These etch rates are generally independent of processing conditions as long as the film maintains a Si-to-C ratio of close to unity. Like other properties, the optical bandgap of amorphous SiC ranges between 1.8 and 3 eV depending on deposition conditions [192].

2.3.13.2 Process Selection Guidelines

Tables 2.54 and 2.55 summarize the material properties and associated deposition processes for PECVD SiC films.

2.3.13.3 Case Studies

As mentioned previously, residual stress can be a significant issue with SiC films deposited by PECVD. If the substrate temperature is kept at or below 400°C (the typical high setpoint on substrate heaters in commercial PECVD systems) the resulting films are amorphous and likely hydrogenated. Sarro et al. were among the first to systematically investigate the use of amorphous SiC films deposited by PECVD for micromechanical structures [200]. They used a Novellus Concept One™ PECVD system that was equipped with low- and high-frequency power supplies. The deposition temperature was held constant at 400°C and initial depositions were performed at 2.25 torr, a SiH_4 gas flow of 100 sccm, and a CH_4 gas flow of 300 sccm. The RF power was 1000 W divided equally between the low-frequency and high-frequency supplies. They found that the resulting residual stress was about –600 MPa. Experiments in varying the low-frequency component showed that films with –2 MPa of stress could be deposited with a low-frequency power of 0 W, but at a cost to thickness uniformity and deposition rate. Annealing at 600°C in nitrogen is sufficient to shift the residual stress into the tensile region.

In a follow-on study this group investigated the effect of substrate material on the residual stress in PECVD SiC films [204]. They found that for PECVD SiC films deposited under the same set of conditions, films deposited on thermal oxides had the lowest residual stress (10 MPa), and those deposited on PSG had considerably higher residual stresses, ranging from 169 MPa for a PSG layer with 2% phosphorus to 218 MPa for a PSG layer with 8% phosphorus. Moreover, doped SiC films on thermal oxides had a much higher residual stress than their undoped counterparts, measuring 177 and 367 MPa for phosphorus- and boron-doped SiC, respectively. The same doped films deposited on PSG with 4% phosphorus had residual stresses of 262 and 449 MPa for phosphorus- and boron-doped SiC, respectively.

The relatively low deposition temperatures associated with PECVD SiC make it potentially compatible with non-conventional substrate materials like high temperature polymers. Pakula et al. have recently demonstrated that polyimide PI2610™ can be used as a sacrificial layer to form surface micromachined PECVD SiC structures [199]. PI2610™ was selected because it is spin castable, patternable by plasma etching, and has a glass transition temperature above 400°C. In fact, it can be cured at 400°C. Amorphous SiC films were deposited in a Novellus Concept One™ system at a substrate temperature of 400°C, a SiH_4 flow rate of 250 sccm, a CH_4 flow rate of 3 slm, a pressure of 2 torr, a high-frequency power of 450 W and a low-frequency power of 150 W. Under these conditions, the as-deposited films do not require a postdeposition annealing step for stress relaxation because the average residual stress is 65 MPa. This group was able to demonstrate the utility of this capability by successfully fabricating a surface micromachined capacitive pressure sensor. The advantage that polyimide offers over other viable sacrificial materials

Table 2.54 Mechanical properties of SiC films deposited by PECVD[a]

References	Temp (°C)	Gas	Gas flow (sccm)	Pressure (torr)	Power (W)	Dep. rate (nm/min)	Young's modulus (GPa)	Residual stress (MPa)	Hardness (GPa)
[193]	200	$C_6H_{18}Si_2$	1000	0.375		53		–500	
	250	Ar				40		–600	
	300					27		–750	
[194]	300	$C_6H_{18}Si_2$					180	–750	
[195]	300	SiH_4	20	1	HF: 300			–450	
		CH_4	400		LF: 300				
[196]	320	SiH_4	3.6		20			–445	
		CH_4	14.0						
[197]	320	SiH_4	3.6				21–36	–93 to –356	
		CH_4	8.4–32.4						
[198]	350	SiH_4 [b]	2840	1.6	HF: 100		56	–80 to 16	8.8
		CH_4	1440		LF: 100–150				
[199][c]	400	SiH_4	250	2	HF: 450			65	
		CH_4	3000		LF: 150				
[200]	400	SiH_4	100	2.25	HF: 500	67		–350	
		CH_4	3000		LF: 500				
[201]	400	SiH_4	70	1.6	HF: 600	180		–5	
[202]		CH_4	500						
		Ar	700						
[203]	350	$(CH_3)_3SiH$ in He	38	160	HF: 400 LF: 100		75	–150	

[a]Film thickness range: 2–4 μm
[b]2% in Ar
[c]Substrate: polyimide

Table 2.55 Electrical properties and chemical resistance of SiC films deposited by PECVD

References	Temp (°C)	Gas	Gas flow (sccm)	Press (torr)	Power (W)	Dep. rate (nm/min)	Thickness (μm)	Resistivity (Ω cm)	Etch rate (nm/h)
[195]	300	SiH_4	20	1	HF: 300		1	10^7	HF: <1
		CH_4	400		LF: 300				KOH: 1.3
									HF/HNO_3: 10.5
[201]	400	SiH_4	70	1.6	HF: 600	180	1.8		HF: 1
[202]		CH_4	500						KOH: 78
		Ar	700						

such as SiO_2 is that the release step can be performed using an isotropic oxygen plasma, thus enabling the integration of such structures directly onto Si CMOS substrates.

2.3.14 PECVD Carbon-Based Films

2.3.14.1 Material Properties and Process Generalities

Diamondlike carbon films are commonly used in non-MEMS applications requiring materials that can withstand high mechanical wear conditions due to their high hardness properties. DLC is typically deposited by PECVD using a hydrocarbon precursor such as methane. DLC has been used as a structural material in MEMS, but the instances are limited, most likely due to high residual stresses in as-deposited films. DLC is more likely to be used as a protective coating for MEMS components, especially polysilicon actuators subject to mechanical wear [205, 206] and stiction [206] owing to its outstanding tribological properties and relatively benign surface chemistry.

2.3.14.2 Process Selection Guidelines

Table 2.56 summarizes the process-dependent properties of DLC films deposited by PECVD. The body of work in developing PECVD diamondlike carbon films is much more extensive than is represented here because the preponderance of the work has been for applications other than MEMS. The references in Table 2.56 were included in this chapter because they describe the development of DLC specifically for MEMS applications.

Table 2.56 Mechanical properties of diamondlike carbon films deposited by PECVD

References	Gas	Gas flow (sccm)	Power (W)	Bias voltage (V)	Pressure (torr)	Young's modulus (GPa)	Tensile strength (GPa)	Residual stress (MPa)
[207]	C_6H_6	na	700	100–500	10	16–133		400–1200
[208]	C_6H_6	na	800	400	10	87		–1300
[209]	CH_4	14	900–1100	375–400	0.02	35	0.12–0.9	–79 to –310
	H_2	42						

2.4 Epitaxy

2.4.1 Process Overviews

Epitaxy is a special case of thin-film growth where a single-crystalline thin-film is grown upon a single-crystalline substrate such that the crystalline structure of the film is formed using the crystalline structure of the substrate as a template. If the substrate and thin-film are of the same material, the process is known as homoepitaxy. If the substrate and thin film are of different materials, the process is known as heteroepitaxy. Epitaxial processes are not commonly used in Si-based MEMS, perhaps because most MEMS structures simply do not require thin single crystalline structures, and the ones that do can be fabricated using silicon-on-insulator (SOI) substrates. In some material systems, however, epitaxial films are extensively used. These include cubic silicon carbide (3C-SiC) on silicon substrates, III-V compounds on III-V substrates and, to a lesser extent, GaN on silicon substrates. In such cases, the film growth processes very closely resemble those developed for microelectronics where single-crystalline structures are a necessity.

From a first principles perspective, the film-forming mechanism associated with epitaxial growth can be described by a simple two-dimensional (2-D) growth model. Like the 3-D model that describes the formation of polycrystalline and amorphous films, the 2-D model involves the adsorption, surface migration, and reaction of vapor-phase reactants on the substrate surface. For epitaxial growth, this substrate must be single crystalline. Epitaxial growth does not require that the surface be atomically flat, just single crystalline. In fact, all single crystalline substrates are comprised of terraces that form steplike structures on the substrate surface with each terrace being comprised of one or more crystalline planes. It is these terraces that greatly facilitate epitaxial growth. Adsorbed reactants, at this stage of the process known as adatoms, migrate on the surface until they come to the edge of a terrace. Once there, the adatom forms a chemical bond with atoms in its vicinity using the crystalline structure on the surface and the terrace edge as a template. This process continues in a highly controlled manner, adatom by adatom, layer by layer, until the desired film is formed.

From the processing perspective, the epitaxial process must be performed under steady-state conditions, which requires tight control of key process parameters. The key distinguishing feature of the epitaxial process when compared with polycrystalline growth is surface migration of the adatoms. If surface migration is encumbered, then 3-D nucleation and growth is likely to occur, resulting in the formation of a polycrystalline or amorphous film. Encumbrance occurs because the surface lacks sufficient energy to sustain epitaxial growth, and this can occur for a number of reasons including excessive adsorption of reactants on the substrate or insufficient surface energy of the newly formed adatoms. The adsorption rate can be properly controlled by regulating precursor flow rates into the reactor and the adatom surface energy can be maintained by performing the growth process at high temperature. For example, polysilicon films are typically grown at temperatures around 600°C whereas epitaxial silicon films are grown at temperatures in excess of

1000°C. Likewise, poly-SiC films are deposited in the 800–900°C range, whereas epitaxial silicon carbide films are grown at temperatures in excess of 1200°C.

Most epitaxial semiconductor films are grown by a process called vapor phase epitaxy (VPE). VPE is essentially a special form of CVD. VPE can be performed at either low pressures or atmospheric pressure and thus follows the appropriate discussions on the topic as presented in previous sections of this chapter. Because of the high temperatures associated with Si and SiC epitaxy, atmospheric pressure CVD is often employed, although LPCVD can be used enabling epitaxial growth to occur at lower temperatures. VPE also works well for Si and SiC because the gaseous precursors required for film growth are readily available. These include SiH_4 and SiH_2Cl_2 for silicon sources and C_3H_8 for the carbon source. VPE also readily supports in situ doping of Si and SiC using PH_3 and B_2H_6 for silicon epitaxy and NH_3 and trimethyl aluminum ($Al(CH_3)_3$) for SiC.

Non-silicon-containing compound semiconductors, such as the III-V semiconductors can also be epitaxially grown by VPE. Sometimes known as MOCVD, short for metallorganic CVD as a result of the metal containing organic precursors used in the process, the process is commonly used to grow binary, ternary, and quaternary III-V compounds on GaAs and InP substrates. Common precursors include arsine and phosphine in conjunction with metallorganics such as trimethyl aluminum and trimethyl gallium.

Epitaxy is not limited to CVD, in fact, methods based on physical vapor deposition (PVD) are also commonly used to grow binary, ternary, and quaternary III-V compound semiconductors, the most popular being molecular beam epitaxy (MBE). The typical MBE system uses “atomic” or “molecular beams” that are thermally generated from discrete sources which are directed at a heated substrate. The flux of atoms or molecules from each source is regulated by control of the source heater, and the beam can be terminated altogether by shuttering the source. The process is performed in a chamber capable of achieving ultrahigh vacuum conditions (10^{-11} torr) in order to maintain conditions for high-purity epitaxial growth. Growth rates tend to be much lower than for CVD methods, however, complex multilayered ultrathin-film stacks, known as superlattices, can readily be grown using MBE. In addition to III-V based films, MBE can be used to grow epitaxial Si, SiGe, and even 3C-SiC films.

2.4.2 Epi-Polysilicon

2.4.2.1 Material Properties and Process Generalities

Some device designs require polysilicon thicknesses that are not easily achieved using conventional LPCVD. In such instances, epitaxial Si reactors can be used to grow polysilicon films. Unlike conventional LPCVD processes that typically have deposition rates less than 10 nm/min, epitaxial processes have deposition rates on the order of 1 μm/min [210]. The high deposition rates result from the much higher substrate temperatures (>1000°C) and deposition pressures (>50 torr) associated with epitaxial processes. Known as epitaxial polysilicon or simply epi-poly, these

Table 2.57 Deposition conditions and mechanical properties for epi-poly films

References	Temp (°C)	Gas	Gas flow (sccm)	Dep. rate (μm/min)	Thickness (μm)	Fracture strength (GPa)	Residual stress (MPa)	Stress gradient (MPa/μm)
[213]	1000	DCS	750–1050	0.55–0.75	10		–25 to 3	
[211]	1000	DCS	1050	0.5	10	0.76	3	2
		PH_3	5%					
[214]	1000	DCS						
		PH_3	5%		10	1	8	1
[210]	1050	DCS	360	~1	4		Low tensile	
[215]	1080	$SiCl_4$	15 g/min	~1			Low tensile	
		H_2	200 slm					

films exhibit many of the properties associated with LPCVD polysilicon but at much higher thicknesses due to the higher growth rates.

Unfortunately, the high growth temperatures associated with epi-poly generally leads to delamination of the films when SiO_2 is used as a substrate layer. This issue can be addressed by using a thin LPCVD polysilicon film as a seed layer for epi-poly growth. In addition to improving adhesion, the LPCVD polysilicon seed layer is sometimes used in order to control nucleation, grain size, and surface roughness.

As with conventional polysilicon, the microstructure and residual stress of the epi-poly films is related to deposition conditions. Compressive films generally have a mixture of <110> and <311> oriented grains [211, 212] and tensile films have a random mix of <110>, <100>, <111>, and <311> oriented grains [213]. The Young's modulus of epi-poly measured from micromachined test structures is comparable with LPCVD polysilicon [212].

2.4.2.2 Process Selection Guidelines

Details regarding the deposition of epi-poly films can be found in Table 2.57. Annealing is generally not required due to the fact that the films are grown at high substrate temperatures; however, if the films are doped, a postdeposition anneal is sometimes performed. Table 2.58 describes details regarding such anneals.

2.4.2.3 Case Studies

Epi-poly films are deposited at temperatures comparable to thermal oxidation temperatures (>1000°C) which, at first pass, might lead the process engineer to assume that these films should be stable from the perspective of mechanical properties, at elevated temperatures. In an effort to evaluate the compatibility of epi-poly with bipolar and CMOS processing, Gennissen et al. studied the sensitivity of various aspects of epi-poly films to high-temperature processing steps associated with bipolar electronics processing [210]. As with nearly all other reports on epi-poly

Table 2.58 Annealing behavior of $POCL_3$ doped epi-poly films

References	Temp (°C)	Gas	Thickness (μm)	Young's modulus (GPa)	Fracture strength (GPa)	Residual stress (MPa)	Annealing conditions	Stress gradient (MPa/μm)
[212]	1150		11.5	160–167	∼1.2	–10	1100°C, 7 h	
[216]	1150	DCS[a]	11				N_2, 1100°C, 7 h O_2 1000°C, 0.5 h	–0.11

[a]DCS: Dichlorosilane (SiH_2Cl_2)

processing, they used a polysilicon seed layer to promote growth of epi-poly on oxide-coated wafers. They found that only thermal oxides were suitable as sacrificial layers for epi-poly processing because LTO and PSG lacked the thermal stability to survive growth even with the LPCVD polysilicon seed layer. They reported that LTO suffers from delamination whereas PSG suffers from outgassing, causing bubbles in the polysilicon layer. As for the high-temperature stability of epi-poly films, specimens subjected to oxidative conditions at high temperature (∼1100°C) acquire a high degree of compressive strain relative to unexposed films as well as films exposed to high temperatures in an argon environment. The authors ascribe the increased strain to oxygen diffusion into the epi-poly film. It was shown that a nitride capping layer commonly used in the LOCOS process is sufficient to protect the epi-poly films from the adverse affects of oxidation.

The fact that epi-poly does not readily nucleate on SiO_2 surfaces has recently been exploited in a selective growth process for patterning epi-poly films [215]. The process is simple in concept: namely grow epi-poly films on patterned LPCVD polysilicon seed layers. Nucleation is inhibited in the large oxide field areas between patterned polysilicon structures. The growth rate of epi-poly from the sidewalls of the patterned polysilicon seed layer is approximately equal to the vertical growth rate, resulting in significant widening of the final structure as compared with the seed layer; however, for larger MEMS structures, this can be accounted for during process design and mask development. The selective growth process eliminates the need to use deep reactive ion etching to pattern thick (>15 μm) epi-poly films.

2.4.3 Epitaxial Silicon Carbide

2.4.3.1 Material Properties and Process Generalities

SiC thin films can be grown or deposited using a number of different techniques. For high-quality single-crystal films, APCVD and LPCVD processes are most commonly employed. Homoepitaxial growth of 4H- and 6H-SiC yields high-quality films suitable for microelectronic applications but typically only on substrates of the

same polytype. These processes usually employ dual precursors, such as SiH_4 and C_3H_8, and are performed at temperatures ranging from 1500 to 1700°C. Epitaxial films with p-type or n-type conductivity can be grown using aluminum and boron for p-type films and nitrogen and phosphorus for n-type films. Nitrogen is so effective at modifying the conductivity of SiC that growth of undoped SiC films is extremely challenging because the concentrations of residual nitrogen in typical deposition systems are sufficient for n-type doping.

APCVD and LPCVD can also be used to deposit 3C-SiC on Si substrates. Heteroepitaxy is possible despite a 20% lattice mismatch because 3C-SiC and Si have the same lattice structure. The growth process involves two key steps. The first step, called carbonization, converts the near surface region of the Si substrate to 3C-SiC by simply exposing it to a hydrocarbon/hydrogen mixture at high substrate temperatures (>1200°C). The carbonized layer forms a crystalline template on which a 3C-SiC film can be grown by adding a silicon-containing gas to the hydrogen/hydrocarbon mix. The lattice mismatch between Si and 3C-SiC results in the formation of crystalline defects in the 3C-SiC film, with the density being highest in the carbonization layer and decreasing with increasing thickness. The crystal quality of 3C-SiC films is nowhere near that of epitaxially grown 4H- and 6H-SiC films; however, the fact that 3C-SiC can be grown on Si substrates enables the use of Si bulk micromachining techniques to fabricate a host of 3C-SiC-based mechanical devices including microfabricated piezoresistive pressure sensors [217]. For designs that require electrical isolation from the substrate, 3C-SiC devices can be made directly on SOI substrates [218] or by wafer bonding and etchback, such as the capacitive pressure sensor developed by Young et al. [219]. High-quality 3C-SiC films can be grown on Si substrates by molecular beam epitaxy [220], although the process is much less commonly used than APCVD or LPCVD.

The mechanical properties of 3C-SiC are of particular interest to the MEMS community due to their potential in applications requiring a structural material with a high Young's modulus. Owing to its compatibility with silicon micromachining, structures to evaluate the mechanical properties of epitaxial 3C-SiC films, such as micromachined membranes and cantilever beams, can easily be fabricated using a combination of SiC reactive ion etching and Si bulk micromachining. Reported values of Young's modulus for 3C-SiC films vary significantly, from a low of 330 GPa [221] to a high of 694 GPa [222] for 2.7 and 10 μm thick undoped films, respectively. At present, it is not clear if or how the high defect density at the 3C-SiC/Si interface affects these measured values.

2.4.3.2 Process Selection Guidelines

Tables 2.59 and 2.60 summarize the processing data and mechanical properties measurements for epitaxial 3C-SiC films grown by APCVD and LPCVD, respectively.

2.4.3.3 Case Studies

It is generally believed that 3C-SiC films epitaxially grown on Si wafers using the conventional carbonization-based growth process will have tensile residual stresses

Table 2.59 Epitaxial growth conditions and mechanical properties of APCVD 3C-SiC films

References	Temp (°C)	Gas	Gas flow (sccm)	Thickness (μm)	Young's modulus (GPa)	Tensile strength	Residual stress (MPa)
[223]	1280	C_3H_8 (15% in H_2)	26	0.5–2	424	1.65	
		SiH_4 (5% in H_2)	102				
		H_2	25,000				
[224]	1350	C_3H_8	10	3.2			549–639
		SiH_4	1				
		H_2	10,000				
[225]		C_3H_8 (15% in H_2)	26	2	407		275
		SiH_4 (5% in H_2)	102				
		H_2	25,000				

Table 2.60 Epitaxial growth conditions and mechanical properties of LPCVD 3C-SiC films

References	Temp (°C)	Gas	Gas flow (sccm or ratio)	Pressure (torr)	Young's modulus (GPa)	Residual stress (MPa)
[132]	1350	SiH_4	$Si/H_2 = 0.024\%$	300	446	
		C_3H_8	$C/Si = 0.8 - 1$			
		H_2 (98% in Ar)				
[226]	1350	SiH_4 (10% in H_2)	270	400		215–450
		C_3H_8	8			
		H_2	10,000			
[227]	1380	C_3H_8	8	100	430	265
		SiH_4 (10% in H_2)	270			
		H_2	30,000			

in the 200–400 MPa range due to the thermal and lattice mismatches between the film and the substrate. Gourbeyre et al. have shown that the conditions used during the carbonization step play a key role in determining the residual stress in the films [224]. Carbonization is usually initiated by exposing the substrate to the carbonizing precursor at relatively low temperatures (<500°C) then ramping up the substrate temperature to the carbonization/epitaxial growth temperature (>1200°C). They found that the stress in the epitaxial film could be made either tensile or compressive by (1) utilizing a three-step process that decouples the carbonization and epitaxial growth temperatures and (2) properly selecting the temperature at which the carbonization precursor is injected into the reactor. For instance, they found that compressive films are grown when the carbonization precursor is introduced at a substrate temperature of 300°C, carbonization is performed at 1150°C and epitaxial growth at 1350°C, whereas tensile films are grown when the introduction temperature is equal to or greater than 1150°C and carbonization temperature is also equal

to or greater than 1150°C. Using this knowledge, the authors were able to fabricate a freestanding 3C-SiC membrane with a tensile stress of 157 MPa.

2.4.4 III-V Materials and Gallium Nitride

2.4.4.1 Material Properties and Process Generalities

Gallium arsenide (GaAs), indium phosphide (InP) and related III-V compounds have favorable piezoelectric and optoelectric properties, high piezoresistive constants and wide electronic bandgaps relative to Si, making them attractive for various sensor and optoelectronic applications. Like Si, GaAs, and InP substrates are commercially available as high-quality, single-crystal wafers. In addition to the commonly known binary compounds, III-V materials can be deposited as ternary and quaternary alloys with lattice constants that closely match the binary compounds from which they are derived (i.e., $Al_xGa_{1-x}As$ and GaAs), thus permitting the fabrication of a wide variety of heterostructures that facilitate device performance.

GaAs has a zinc blend crystal structure with an electronic bandgap of 1.4 eV, enabling GaAs electronic devices to function at temperatures as high as 350°C [228]. High-quality, single-crystal GaAs wafers are widely available, as are well-developed MOCVD and MBE growth processes for epitaxial layers. Because the epitaxial growth processes used in the fabrication of III-V MEMS come directly from the electronic device industry, the MEMS literature lacks publications that link thin-film deposition details to material properties. Nevertheless, Table 2.61 summarizes important material properties of III-V compounds as measured using MEMS devices.

Interest in gallium nitride (GaN) as a material for MEMS has recently emerged, due to its large bandgap (∼3.5 eV), its piezoelectric properties, and compatibility with 6H-SiC and (111) Si substrates. Epitaxial GaN films can be deposited on both substrate materials using AlN as an intermediate buffer layer. Development of this material is still in its early stage so data pertaining to its mechanical properties are sparse. Table 2.62 summarizes the mechanical properties of epitaxial GaN thin-films as measured using MEMS structures.

2.4.4.2 Process Selection Guidelines

Tables 2.61 and 2.62 detail deposition processes and associated material properties for III-V and GaN films developed specifically for MEMS applications.

2.4.4.3 Case Studies

Micromachining of GaAs is relatively straightforward, because many of the ternary and quaternary alloys used for epitaxial growth have sufficiently different chemical properties to allow their use as sacrificial layers [238]. For example, a commonly

Table 2.61 Mechanical properties of selected III-V semiconductors

References	Material	Substrate	Thickness (μm)	Young's modulus (GPa)	Fracture stress (GPa)	Residual stress (MPa)	Stress gradient (MPa/μm)
[229]	$Al_{0.3}Ga_{0.7}As$ $Al_{0.6}Ga_{0.4}As$	GaAs		107	0.75–1.25		
[230]	InP	$In_{0.53}Ga_{0.47}As$	1.7	82		–5.6	[a]
[231][b]	InP	InGaAs/InP				–100	
[232]	InP	InGaAs/InP					16.32
[233]	InP	$Ga_{0.47}In_{0.53}As$/InP	0.018				∼200
			0.035				∼100
			0.053				∼–100
			0.070				∼–150
			0.105				∼–200
[234]		InGaAs/InP	1	∼80			

[a] This sample exhibited a strain gradient of $4.37 \times 10^{-5}/\mu m$

[b] This sample was bonded to a SiO_2 coated Si wafer for micromachining

Table 2.62 Deposition conditions and mechanical properties of GaN films

References	Substrate	Method	Temp (°C)	Gas	Gas flow (μmol/min)	Pressure (torr)	Thickness (μm)	Young's modulus (GPa)	Residual stress (MPa)
[235]	AlGaN/Si	MBE	800				0.5–1[a]	280	
[236]	AlN/SOI	CVD	1000	TMG[b]	150	100	1.7		440–530
[237]	AlN/Si			NH_3	0.45				810
				H_2					

[a] AlGaN buffer layer thickness = 20 nm
[b] TMG: Trimethyl gallium: $(Ga(CH_3)_3)$

used ternary alloy for GaAs is $Al_xGa_{1-x}As$. For values of x less than or equal to 0.5, etchants containing mixtures of HF and H_2O will remove $Al_xGa_{1-x}As$ without attacking GaAs, whereas etchants containing NH_4OH and H_2O_2 attack GaAs isotropically but do not etch $Al_xGa_{1-x}As$. This selectivity enables the micromachining of GaAs using lattice-matched etch stops and sacrificial layers. GaAs cantilevered structures have also been fabricated on Si wafers [239]. The process involves the growth of a 40 nm thick buffer layer of heteroepitaxial GaAs at 400°C on a (100) Si wafer that was deoxidized in H_2 at 950°C followed by exposure to AsH_3 during the cool-down step once the temperature reaches 850°C. After the buffer layer is grown, the main structural film is grown at 640°C. The GaAs multilayer is patterned using a $HBr:CH_3COOH:K_2Cr_2O_7$ solution at a ratio of 1:1:1. Devices are released by etching the underlying Si wafer in 30% KOH at 60°C. The fracture stress of these structures was measured to be ∼1.5 GPa.

Many of the properties of InP are similar to GaAs in terms of crystal structure, mechanical stiffness, and hardness; however, the optical properties of InP make it particularly attractive for micro-optomechanical devices to be used in the 1.3–1.55 μm wavelength range. Micromachining of InP follows closely that used for GaAs. Like GaAs, single-crystal wafers of InP are readily available and ternary and quaternary lattice-matched alloys, such as InGaAs, InAlAs, InGaAsP, and InGaAlAs, can be used as either etch stop and/or sacrificial layers depending on the etch chemistry [238]. InP thin-films, for example, deposited on $In_{0.53}Al_{0.47}As$ sacrificial layers can be released using etchants containing $C_6H_8O_7$, H_2O_2, and H_2O. In addition, InP films and substrates can be etched in solutions containing HCl and H_2O using $In_{0.53}Ga_{0.47}As$ films as etch stops. InP cantilevers have even been fabricated on Si substrates [240]. The process involves epitaxial growth of InP on (100) Si wafers by MOCVD, followed by patterning of the InP thin-film into cantilevers using a 1:1 solution of HCl and $H_3\ PO_4$. The cantilevers are released by selectively etching the Si substrate in a 30% KOH solution at 60°C. The resulting structure is an InP cantilever with a large Si proof mass near its end. The structure was used to study the fracture characteristics of the InP films.

Indium arsenide (InAs) can also be micromachined into device structures. Despite a 7% lattice mismatch between InAs and (111) GaAs, high-quality epitaxial layers can be grown on GaAs substrates. Yamaguchi et al. developed a process to fabricate very thin conductive membranes of InAs on GaAs substrates [241]. Thin InAs films were grown directly on GaAs substrates by MBE and etched using a

solution containing H_2O, H_2O_2, and H_2SO_4. The structures were released by etching the GaAs substrate using a $H_2O/H_2O_2/NH_4OH$ solution. InAs cantilevers have also been fabricated on GaAs using a $Al_{0.5}Ga_{0.5}Sb$ sacrificial layer [242].

Ternary compounds have also recently been utilized in MEMS structures. For example disk-type microresonators based on epitaxial AlGaAs films have been fabricated [243]. The resonator consists of a surface-micromachined disk that is tethered to the substrate by four supporting beams. The disk is made from a Si-doped $Al_{0.3}Ga_{0.7}As$ layer that clads an undoped $Al_{0.3}Ga_{0.7}As$ layer. This three-layer stack is grown on a sacrificial $Al_{0.7}Ga_{0.3}As$ layer that is epitaxially grown on a commercially available GaAs wafer. The resonator is patterned by reactive ion etching and the device is released in HF.

2.5 Physical Vapor Deposition

2.5.1 Process Overviews

Physical vapor deposition (PVD) is a process by which a physical mechanism is the primary means by which a film-producing vapor is generated (in contrast to CVD where gaseous chemical precursors are used). The most common physical processes include sputtering and thermal evaporation, although alternative methods such as laser ablation are emerging for niche applications. As compared to CVD, PVD is not commonly used to deposit semiconductors and dielectrics for MEMS, although enough examples can be found in the literature to warrant inclusion in this chapter. For a detailed description of PVD, the reader is directed to [1–3].

Thermal evaporation is one of the oldest and most mature vacuum deposition methods. This technique involves the creation of the physical vapor by heating the source material. For materials with relatively low melting temperatures (i.e., polymers and metals such as Al), the source material can be heated using a simple resistive heater such as a tungsten filament. For materials with high melting temperatures (i.e., compounds and metals such as Pt), heating is by electron bombardment. Evaporation is generally performed under high vacuum conditions to ensure chemical purity of the as-deposited film and to minimize gas phase collisions that could lower the kinetic energy of the vapor. Deposition generally does not conform to complex topographies. For MEMS applications, deposition of semiconductors and dielectrics by evaporation is not commonly performed and thus is not reviewed in this chapter.

Sputtering uses ion bombardment of a solid target to generate the physical vapor. Argon gas is commonly used as the ion source because it is relatively easy to ionize, has a relatively high mass, and is chemically inert. The ion beam has an average energy in the keV range, which is sufficient to liberate atoms from most target materials. If the target material is electrically conductive, then a DC bias can be used to accelerate the Ar ions to the target. In contrast, if the material is electrically insulating, an RF bias is required to suppress charge buildup on the target surface.

Elemental semiconductors such as silicon and heavily doped wide-bandgap semiconductors such as SiC can be deposited by DC sputtering. Insulators such as silicon dioxide and undoped SiC can be deposited from targets of the same material by RF sputtering, which serves to suppress charging of the insulating targets. Alternatively, these compounds can be deposited by reactive sputtering, which involves DC sputtering of a Si target in the presence of a reactive gas. For example, sputtering a Si target using methane as the sputtering gas will yield a SiC thin-film. Sputtering is generally performed under high vacuum conditions to ensure chemical purity of the as-deposited film and to minimize gas phase collisions that could lower the kinetic energy of the vapor, although the vacuum conditions tend to be less stringent than for evaporation.

For some materials such as carbon, alternative techniques have been developed, the most notable being pulsed laser deposition. Instead of bombarding a target with an ion beam, laser illumination using extremely short laser pulses (∼ns) is instead used. The incident radiation is absorbed in the near surface region of the target, resulting in highly localized heating and vaporation of target material. Process control is achieved through the laser pulse length, pulse repetition rate, and substrate heating. This approach enables the process to be performed at lower vacuum levels than conventional PVD because a sputtering gas is not required. The technique is not well suited for producing thick films, but can be used to produce thin-films such as those to be used as protective coatings.

2.5.2 Sputter-Deposited Si

2.5.2.1 Material Properties and Process Generalities

PVD techniques have been developed to produce Si thin films [244, 245] as a low temperature alternative to LPCVD polysilicon and PECVD amorphous silicon. Abe and Reed showed that sputtering could be used to deposit very smooth (2.5 nm) polysilicon films on thermally oxidized wafers at reasonable deposition rates and with low residual compressive stresses [244]. The process involved DC magnetron sputtering from a Si target using an Ar sputtering gas, a chamber pressure of 5 mtorr, and a power of 100 W. The authors reported that a postdeposition anneal at 700°C in N_2 for 2 h was needed to crystallize the deposited film and perhaps lower the stress. Honer and Kovacs developed a polymer-friendly, Si-based surface micromachining process based on polysilicon sputtered onto polyimide and PSG sacrificial layers [245]. To improve the conductivity of the micromachined Si structures, the sputtered Si films were sandwiched between two TiW cladding layers. Devices fabricated on polyimide sacrificial layers were released using oxygen plasma etching. The processing step with the highest temperature was in fact, the polyimide cure at 350°C. To test the robustness of the process, sputter-deposited Si microstructures were fabricated on substrates containing CMOS devices. As expected, the authors reported no measurable degradation of device performance. Pal and Chandra found that sputtered Si films deposited at a substrate temperature of ∼250°C are amorphous

Table 2.63 Deposition conditions and material properties of Si films deposited by sputtering[a]

Reference	Substrate	Power (kW)	Pressure (mtorr)	Dep. rate (nm/min)	Thickness (nm)	Residual stress (MPa)	Resistivity (MΩ/sq)
[245]	Si	1.5	8	23		34	
	Si	1.5	14	19		141	
	PSG	1.5	8	23		97	
	PSG	1.5	14	19		106	
	Al/Si	1.5	8	23		31	
	Al/Si	1.5	14	19		109	
	Si	2.5	8	37		–22	
	Si	2.5	14	30		164	
	PSG	2.5	8	37		27	
	PSG	2.5	14	30		13	
	Al/Si	2.5	8	37		–16	
		2.0	9.5		600	∼90	50
			9.5		2000	∼98	20
			9.5		5000	∼105	7

[a]Deposition temperature: room temperature

Table 2.64 Mechanical and electrical properties of annealed Si films deposited by sputtering

References	Power (kW)	Pressure (mtorr)	Thickness (nm)	Annealing temp (°C)	Residual stress (MPa)	Resistivity (MΩ/sq)	Strain (10^{-5})
[245]	2.0	9.5	600	350	95	125	
		9.5	2000		68	20	
		9.5	5000		70	6	
[244]	0.10	5		700			–5.6 ×

and that an annealing temperature of 800°C is required to induce crystallization [246].

2.5.2.2 Process Selection Guidelines

Table 2.63 details the various processes used to produce sputter-deposited Si films for MEMS applications and Table 2.64 describes the mechanical and electrical properties of sputter-deposited Si films after annealing.

2.5.3 Sputter-Deposited SiC

Sputtering can be used to deposit SiC films on temperature-sensitive substrates. In fact, sputtering is able to produce SiC films at temperatures as low as 25°C. Sputtered SiC films can be deposited by RF magnetron sputtering of a SiC target

[247] or by dual source DC magnetron sputtering of Si and graphite targets [248]. In both cases, the films are amorphous in microstructure and electrically insulating. Because the process does not involve hydrogen-containing precursors, the films consist only of Si and C.

Ledermann et al. developed a process to deposit low-stress (100 MPa), chemically resistant amorphous SiC films by RF magnetron sputtering [247]. Processing details are provided in Table 2.65. The sputtering target was an unspecified stoichiometric SiC target. Argon was used as the sputtering gas. The residual stresses in as-deposited films ranged from moderately tensile to highly compressive dependent on deposition conditions, in particular, chamber pressure, cathode power, and substrate bias [247]. These films retain excellent chemical durability as no degradation was observed in these films when exposed to a 40% KOH solution at 80°C.

Table 2.65 Mechanical properties of SiC films deposited by sputtering

References	Substrate	Temp (°C)	Power (kW)	Pressure (mtorr)	Dep. rate (nm/min)	Thickness (nm)	Residual stress (MPa)	Hardness (GPa)
[247]	Si, SiO_2	RT	0.05–0.3	4–31.95	5–20		100 to –1400	
[248]	Si, glass	RT	0.2	2.25–7.5		100–2000	–61 to 210	18

Inoue et al. developed a sputtering process for SiC films using a dual source approach [248]. In their approach, pure Si (99.999%) and graphite (99.999%) targets were sputtered using ultrahigh-purity Ar gas. Process details are provided in Table 2.65. They found that 2 μm thick films with tensile stresses of nominally 130 MPa could readily be deposited with 50 W of power on the Si cathode and 200 W of power on the graphite cathode. Free-standing membranes of only 100 nm in thickness and suitable for X-ray soft filters were fabricated from these films.

2.5.4 Sputter-Deposited SiO_2

Sputtered SiO_2 films are much like their PECVD counterparts in that they are electrically insulating and amorphous in microstructure. Like sputtered SiC, the deposition temperatures can be as low as 25°C, making them very attractive for backend processes. Residual stresses in as-deposited films can be both compressive and tensile, although the tensile stresses can be excessive. Bhatt and Chandra [249] have developed a sputtering process suitable for the production of micromachined SiO_2 structures. Their process involves RF sputtering of a SiO_2 target at substrate temperatures below 285°C. In fact, no substrate heating was used, but the authors measured a maximum substrate temperature of 285°C during the deposition process. Etch rates of the sputtered SiO_2 films depended on RF power and chamber pressure. It was found that the etch rates in buffered HF ranged from roughly 130 to 750 nm/min. The etch rates in KOH ranged from 3.5 to 5.0 nm/min whereas

that in EPW ranged from 0.25 to 0.6 nm/min. For comparison purposes, the authors reported the etch rates of thermal oxide in equivalent buffered HF, KOH, and EPW solutions to be 110, 3, and 0.2 nm/min, respectively. The authors found that the films were sufficiently mechanically and chemically stable to serve as masking layers for boron diffusion performed at 1050°C. The sputtered films were successfully used as interface layers in Si-to-Si wafer bonding, and free-standing cantilevers and microbridges could be fabricated by surface and bulk micromachining. In the case of the cantilevers, a thin ZnO film was used as the sacrificial layer. Table 2.66 provides process details for the sputtered SiO_2 films in [249].

Table 2.66 Deposition conditions and properties of silicon dioxide films deposited by sputtering [249]

Substrate	Temp (°C)	Power (kW)	Pressure (mtorr)	Dep. rate (nm/min)	Thickness (nm)	Residual stress (MPa)	Surface roughness (nm)
Si, quartz	25–285	0.1– 0.3	5–20	40–180	500	–90 to 3000	0.2–3.6

2.5.5 Sputter-Deposited Diamondlike Carbon

Sputter deposition of carbon films is not commonly used in MEMS fabrication but can be performed if films with high hardness and moderate resistivity are required. The films have a much lower Young's modulus value than polycrystalline diamond, but they can be deposited at much lower deposition temperatures. Unfortunately, residual stresses in these films are excessive thus limiting their utility. Table 2.67 summarizes the deposition conditions and observed mechanical properties for a DLC film developed for MEMS applications.

Table 2.67 Deposition conditions and properties of diamondlike carbon films deposited by sputtering[a] [250]

Temp (°C)	Power (kW)	Pressure (torr)	Dep. rate (nm/min)	Thickness (nm)	Residual stress (MPa)	Young's modulus (GPa	Resistivity (Ω cm)	Hardness (GPa)
100	1.5	3.75	5–20	500	2000	200	0.2	30

[a] Gauge Factor = 20

2.5.6 Carbon Films Deposited by Pulsed Laser Deposition

Pulsed laser deposition is an alternative deposition method to CVD-based techniques for diamond MEMS. The process is performed in a high vacuum chamber and uses a pulsed eximer laser to ablate a pyrolytic graphite target. Material from

the ejection plume deposits on a substrate, which is kept at room temperature. Background gases composed of N_2, H_2, and Ar can be introduced to adjust the deposition pressure and film properties. The as-deposited films consist of tetrahedrally bonded carbon that is amorphous in microstructure, hence the name amorphous diamond. Nominally stress-free films can be deposited by proper selection of deposition parameters [251] or by a short postdeposition annealing step [252]. The amorphous diamond films exhibit many of the properties of single-crystal diamond, such as a high hardness (88 GPa) a high Young's modulus (1100 GPa), and chemical inertness. Surface micromachined structures can be fabricated using these films; in part because the films can readily be deposited in oxide sacrificial layers and can be etched in an oxygen plasma. Cho et al. report a Young's modulus of 759 GPa and a tensile strength of 7.3 GPa for carbon films deposited by KrF eximer laser PLD [253]. Table 2.68 details the mechanical properties of diamondlike carbon films deposited by PLD for MEMS applications

Table 2.68 Mechanical properties of diamondlike carbon films deposited by pulsed laser deposition[a,b]

References	Target	Power (J/cm^2)	Pressure (μtorr)	Young's modulus (GPa)	Tensile strength (GPa)	Residual stress (MPa)	Hardness (GPa)
[251]	Graphite		1	759	7.3		
[252]	Graphite	>100		550		<–200	80

[a]Deposition conditions: Kr eximer laser
[b]Film thickness range: $1 - 2\,\mu$m

2.6 Atomic Layer Deposition

2.6.1 Process Overview

Atomic layer deposition (ALD) is a variant of CVD where compound materials, typically binary compounds, are formed on a substrate surface by sequential exposure to two highly reactive vapor-phase chemical precursors. Unlike the formation of compounds by conventional CVD where the precursors are introduced to the reaction chamber en masse and film growth occurs simultaneously, in ALD, the substrate is exposed to only one precursor at any given moment. The exposure periods are kept intentionally short so that submonolayer coatings of the adsorbed precursor are formed on the substrate. The two precursors are selected such that they have a high reactivity with each other. The process involves exposure of the substrate to the first precursor, which contains one component of the binary compound, followed by exposure to the second precursor, which contains the second component. Reaction of the first component with the second results in the formation of the desired material as well as the desorption of unwanted by-products. Deposition rates are often

expressed in terms of nm/cycle, where one cycle is complete after the two precursors have reacted following the second exposure period. In between each exposure period, the reaction chamber is purged of chemical precursors to inhibit gas phase reactions. The amount of precursor introduced into the reaction chamber is highly regulated to ensure that the surface reactions are self-limiting and that both precursors are fully reacted in one deposition cycle. ALD is particularly well suited for depositing metal oxide thin-films because many are contained in reactive metallorganic precursors which readily react with oxidants such as water vapor to form metal oxide. ALD is becoming increasingly popular in the development of next generation MOS-based ICs where alternative dielectrics to SiO_2 are being developed. For MEMS applications, the most common material is Al_2O_3, due in large measure to its convenient metallorganic precursor (trimethyl aluminum) combined with the fact that aluminum oxide can easily be formed by reaction of this precursor with water vapor at relatively low temperature.

2.6.2 Process Selection Guidelines and Material Properties

ALD is a relatively new deposition technique that has not yet found widespread use in MEMS technology due to the ultrathin-films that are typically produced by this method. However, the very high degree of conformality associated with the technique combined with the fact that metal oxides such as alumina are highly durable from both chemical and mechanical perspectives make it extremely attractive as a method to apply thin protective coatings on prefabricated MEMS components. Hoivik et al. showed that alumina films deposited by ALD can overcoat all exposed surfaces of a released surface micromachined polysilicon cantilever, albeit with a small variation in thickness between the top and bottom surfaces of the beam [254]. Yang and Kang investigated the chemical durability of ALD alumina films in aqueous and vapor phase HF and found that the films were much more chemically stable when exposed to vapor phase HF than when exposed to aqueous solutions [255]. As development of ALD is in its early stages relative to alternative deposition methods, much is yet to be learned about the MEMS-centric process-related properties of the as-deposited films. Tables 2.69, 2.70, 2.71, and 2.72 summarize much of what has been reported in the literature on the topic.

In addition to the deposition of metal oxides, ALD can also be used to deposit thin single-crystalline films. Known as atomic layer epitaxy, or ALE, this technique is not commonly used in MEMS due in large part to competing methods that are much better suited for producing films thick enough for most MEMS applications. In the case of silicon carbide, however, there is one example in the literature where ALE was used to grow single-crystalline 3C-SiC films for MEMS. Table 2.73 summarizes the findings of this study.

Tables 2.69, 2.70, and 2.71 detail processing conditions and resulting material properties for Al_2O_3 films deposited by ALD. Table 2.73 describes the mechanical properties of ZnO films deposited by ALD and Table 2.73 lists the measured mechanical properties of 3C-SiC films grown by ALE.

Table 2.69 Friction properties of Al_2O_3 films deposited by atomic layer deposition

References	Temp (°C)	Gas	Gas flow Cycle (s)	Pressure (torr)	Dep. rate (nm/cycle)	Thickness (nm)	Coefficient of friction
[256]	168	TMA[a]	1	1	0.101	10	0.3
		H_2O	1				
		N_2	5				
[257]	300–350	WF_6	2	2		10–30	0.008 on SiO_2
		H_2S	2				0.047 on Ni
		N_2	5				

[a]TMA: trimethyl aluminum: $(Al(CH_3)_3)$

Table 2.70 Mechanical properties of Al_2O_3 films deposited by atomic layer deposition

References	Temp (°C)	Gas	Gas flow cycle	Pressure (torr)	Dep. rate (nm/cycle)	Thickness (nm)	Young's modulus (GPa)	Hardness (GPa)	Residual stress (MPa)
[258]	100	TMA[a]	28 s		10		150	8.1	
		H_2O							
		N_2							
	177	TMA	12 s		12		180	12	
		H_2O							
		N_2							
[259]	130	TMA	na			80			258
		H_2O	na						
		N_2	na						
[260]	177	TMA	1 s	1		100–300	168–182		383–474
		H_2O	1 s						
		N_2	5 s						

[a]TMA: trimethyl aluminum: $(Al(CH_3)_3)$

Table 2.71 Electrical properties of Al_2O_3 films deposited by atomic layer deposition

Reference	Temp (°C)	Gas	Gas flow Cycle (s)	Dep. rate (nm/cycle)	Young's modulus (GPa)	Hardness (GPa)	Dielectric constant	Resistivity (Ω cm)
[258]	100	TMA[a]	28	10	150	8.1	6.8	10^{16}
		H_2O						
		N_2						
	177	TMA	12	12	180	12	6.8	10^{16}
		H_2O						
		N_2						

[a]TMA: trimethyl aluminum: $(Al(CH_3)_3)$

2.7 Spin-On Films

Spin-on dielectrics, such as siloxane-based spin-on glass (SOG), have become a mainstay material of backend processing in IC fabrication because the material can be conveniently deposited and processed at reasonable temperatures, and it retains acceptable dielectric properties for surface passivation and mechanical protection of electronic interconnects. SOG is also attractive for MEMS applications because it

Table 2.72 Mechanical properties of ZnO films deposited by atomic layer deposition

Reference	Temp (°C)	Gas	Flow cycle (s)	Pressure (torr)	Dep. rate (nm/cycle)	Thickness (nm)	Young's modulus (GPa)	Hardness (GPa)	Residual stress (MPa)
[258]	100	DEZ[a] H_2O N_2	28		19		134	6	
	177	DEZ H_2O N_2	12		20		143	9	

[a]DEZ: diethylzinc: ($Zn(CH_2CH_3)_2$)

Table 2.73 Mechanical properties of 3C-SiC films grown by atomic layer epitaxy[a]

References	Temp (°C)	Gas	Gas flow (sccm)	Pressure (torr)	Thickness (μm)	Young's modulus (GPa)	Residual stress (MPa)	Resistivity (Ω cm)
[117] [118]	1050	SiH_2Cl_2 C_2H_2	10 10	0.15	0.7–2	347	100–200	0.2

[a]The cycle time per precursor is 5 s. The purge period is 3 s. The growth rate per cycle is 0.9 nm

offers the opportunity to create thick oxide structures that would otherwise be difficult to realize using CVD or PVD methods. Processing of SOG basically involves spin casting the precursor in much the same manner as photoresist is cast, followed by a series of postdeposition thermal bakes. Although the processing conditions vary depending on the source of SOG, the following sequence is representative of a common SOG known as Honeywell Accuglass 512B^{TM} [261].

1. Clean the silicon substrate by immersion for 2 min in a H_2SO_4 and 30% H_2O_2 solution mixed to a 7-to-3 ratio and heated to 120°C.
2. Dip the silicon substrate in a 2.5% HF solution for 2 min.
3. Apply the SOG by spin coating at a rate of 3000 rpm for 10 s.
4. Subject the substrate to a bake at 80°C for 1 min
5. Subject the substrate to a bake at 150°C for 1 min
6. Subject the substrate to a bake at 250°C for 1 min
7. Subject the substrate to a final curing bake at 425°C for 30 min in a flow of N_2 at 1 slm.

In addition to its principle function as a low-temperature material for electrical isolation, SOG has been used in situations where thick sacrificial layers are required. For instance, SOG has been used as a thick film sacrificial molding material to pattern thick polysilicon films [262]. In this example, 20 μm thick SOG films were patterned into molds and filled with 10 μm thick LPCVD polysilicon films, planarized by selective CMP, and subsequently dissolved in a wet etchant containing HCl, HF, and H_2O to reveal the patterned polysilicon structures. The cured SOG films were completely compatible with the LPCVD process and posed

no contamination risk. SOG has also been used as a structural material in high-aspect-ratio channel plate microstructures [263]. Electroplated nickel (Ni) was used as a molding material, with the Ni channel plate molds fabricated using a conventional LIGA process. The Ni molds were then filled with SOG, and the sacrificial Ni molds were removed in a reverse electroplating process. In this case, the fabricated SOG structures were over 100 μm tall by virtue of the LIGA patterned Ni molds.

Casting processes are not limited to SOG; in fact, SiC-based structures have been fabricated using polymer precursors in conjunction with micromolding [264]. This technique uses SU-8 photoresists for the molds. Detailed later in this book, SU-8 is a versatile photodefinable polymer in which thick films (hundreds of microns) can be patterned using conventional UV photolithographic techniques. After patterning, the molds are filled with the SiCN-containing polymer precursor, lightly polished, and then subjected to a multistep heat-treating process. During the thermal processing steps, the SU-8 mold thermally decomposes and the SiCN structure is released. The resulting SiCN structures retain many of the mechanical and chemical properties of stoichiometric SiC.

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