Ion Beams in Nanoscience and Technology

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High Speed Electronics

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1 Introduction

There is no question about the tremendous impact of the micro- and nanoelectronic technology on the world economy and welfare. Since the introduction of the integrated circuit about 40 years ago, the performance has followed a steady scaling outlined already in 1965 by Gordon Moore [1]. What is fascinating to note is that the most commonly produced human artefact today is the transistor. Each year we produce more than 10^{18} transistors, which is more than all printed characters each year in all books, magazines, and newspapers in the world. Most amazingly, the price per transistor is lower than the price per printed character in common magazines. We also see that this furious development will continue with unbroken momentum at least another decade. Market forecasts indicate that the gross world product in 2010 will be approximately $1000 billion.

The semiconductor device technology has met many sceptical comments about hitting the final roadblocks. Every time, new solutions have been presented, and even more revolutionary fabrication and device design methods. Are we close to meeting a fundamental limit as the technology approaches the 22 nm node? Are we running out of atoms? Let's assume a transistor with a gate length of 22 nm and a width of 100 nm; the number of dopant atoms is around ten! Is this possible to control? Yes indeed, since the carrier transport occurs in a slab of inverted charges controlled by the gate potential [2–4].

1.1 Technology Trends for High Speed Electronics

In this section we will present technology trends for high speed electronics, with focus on silicon technology, and discuss the predictions in the International

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Technology Roadmap for Semiconductors (for short, ITRS roadmap). The performance of both complementary metal oxide semiconductor (CMOS) and silicon-germanium (SiGe) bipolar/CMOS (BiCMOS) [5] has been significantly improved in the last 5–10 years. CMOS is now the main choice for radio frequency (RF) integrated circuits, and SiGe BiCMOS has demonstrated record performance in terms of gate delay and cut off frequencies and has recently reached into the half-terahertz domain [6, 7]. In fact, SiGe devices have similar performance as traditional high-speed devices in III–V semiconductor materials, such as InP based heterojunction bipolar transistors (HBTs) or high electron mobility transistors (HEMTs). This can be explained by improved materials—carbon doped SiGe, self-aligned technology with minimized parasitic resistances and capacitances, use of advanced lithography, etc. The evolution of SiGe BiCMOS over four different technology generations is illustrated in Fig. 1.

For CMOS, the gate length scaling is the driving force, which results in improved RF performance. Other improvements such as strained silicon channels, with high carrier mobility, also benefit the RF performance because of the higher intrinsic gain of the MOSFET. Issues related to the voltage scaling are a concern, since a supply voltage of less than 1 V makes it difficult to realize enough voltage swing in an RF/analog circuit. The reliability and breakdown of the thin gate dielectric are also limiting for the RF potential of a highly scaled CMOS. One important advantage of the III–V materials, compared to silicon-based technology, are the well developed optical components such as tunable lasers, which are monolithically integrated with photo detectors and high speed modulators [8]. However, significant progress has been made in silicon CMOS based optoelectronics recently, and an interesting option is hybrid integration of InP, by bonding or epitaxial growth, into the baseline CMOS process. In Sect. 3 below we will discuss some performance boosters such as different types of substrates SOI, and virtual substrates. Strain enhanced mobility is

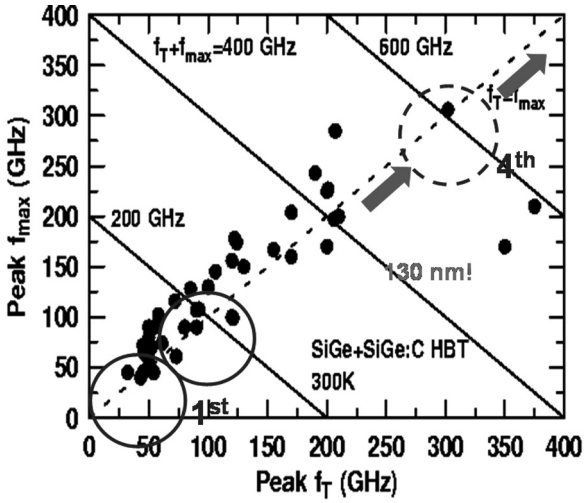

Fig. 1 Example of SiGe performance evolution over four technology generations. Courtesy of John D. Cressler, Institute of Technology, Atlanta, GA [5]

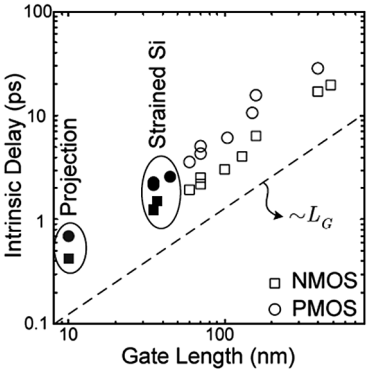

Fig. 2 CMOS performance trends vs. gate length scaling, showing the introduction of strained silicon. Reproduced after Antoniadis et al. [10] with permission from IBM Journal of Research and Development

a very important concept to keep CMOS on the roadmap [9]. Figure 2 illustrates how strain induced mobility enhancement was introduced at about the 90 nm technology node (see the next section for a definition), to ensure continued performance scaling for shorter gate lengths.

To reduce the increasing gate leakage current a paradigm shift, in which the silicon dioxide gate insulator is replaced by a high-κ/metal gate stack was necessary. It should be mentioned that the use of ion beam methods for characterising the κ/metal gate stack is discussed further in chapters "Low and Medium Energy Ion Scattering for Near Surface Structure and Nanoscale Depth Profiling" and "Thin Film Characterisation by Means of MeV Ion Beams". For coming technology nodes, advances in junction technology, both with regard to dopant introduction and to activation, will be crucial.

1.2 International Technology Roadmap for Semiconductors

To illustrate some current trends, we will start by analyzing the predictions by the ITRS roadmap [11]. Here technology evolution is predicted and current roadblocks are highlighted to direct research efforts. The roadmap outlines the key requirements for coming technology generations. In particular, ion implantation (I/I) is covered in the section on front-end process technology and described with device-related parameters such as junction depth (X_j) and extension sheet resistance (R_S). Some difficult challenges are outlined in Table 1 below:

The roadmap uses a metric which refers to the minimum half-pitch of a specific feature, e.g., contacted gates. This is referred to as the technology node. Hence, the roadmap does not define a target gate length as such. Currently, 45 nm technology has been introduced, and the roadmap predictions focus on the upcoming 32 and 22 nm nodes, which are in development. A major paradigm shift took place as high-κ/metal gate was successfully introduced at the 45 nm node. The roadmap states that further reduction of the high-κ dielectric thickness is one of the objectives for coming technology nodes. For the physical gate length, improved control of the

Table 1 Example of front-end process difficult challenges from ITRS 07

Difficult challenges ≥ 22 nm	Summary of issues
Thermal/thin films/doping/etch	Introduction of high-κ/metal gate into high performance and low operating/low standby power and equivalent oxide thickness (EOT) scaling below 0.8 nm Scaling extension junction depths below 10 nm while achieving high dopant activation Gate critical dimension control for physical gate length < 20 nm

critical dimension is required, which includes improved tolerances in the combined lithography and etching steps as well as metrology techniques to measure 20 nm features across a large diameter wafer.

Finally, severe challenges for I/I are anticipated. Achieving 10 nm X_j along with high dopant activation requires very low energy (less than 1 keV) implants and a thermal process which maximizes the dopant activitation, with little or no diffusion. As seen from Table 2 the scaling of X_j will continue, and on a five-year horizon no known solutions are in sight. The same applies to the sheet resistance of the activated extension dopants.

The junction depth issue is controlled by lowering the implantation energy, while the activation is controlled by pre-amorphization or co-implantation of different dopants species. The complexity of the junction formation is therefore significantly increased; a single implanation of one species such as As or B is not sufficient. Ge is used for pre-amorphization and C or F are suggested for co-implantations. There is much interest in diffusionless activation techniques. Among the candidates are laser annealing and solid phase epitaxial regrowth (SPE). In general, annealing times have been reduced, from rapid thermal anneal (RTA)—duration typically 10 s, to spike anneal a fast jump to high temperature (1050–1100 °C, duration 1 s)—immediately followed by fast cool down, and finally millisecond anneal (MSA).

Table 2 Example of predictions in the ITRS roadmap related to dopant introduction

• Year of production	2008	2009	2010	2011	2012
Drain extension Xj (nm)	7.5	7	6.5	5.8	4.5
Maximum allowable parasitic series resistance × width (Ω–μm)	140	120	105	80	70
Maximum drain extension sheet resistance (Ω/sq)	740	677	650	548	593
Extension lateral abruptness for bulk (nm/decade)	2.5	2.2	2	1.8	1.5
Contact Xj (nm)	25.3	22	19.8	17.6	15.4

Color coding: *white/light* and *gray* = solution known, *dark gray* = no known solution. The values refer to bulk MPU/ASIC technology and were obtained from the ITRS 06 update [11]

2 Ion Implantation in High-Speed Device and Integrated Circuit Process Technology

This section outlines the use of I/I in high-speed device and very large scale integrated (VLSI) circuit process technology with a focus on silicon CMOS devices and circuits.

Since the early 1980s, ion implantation has been one of the reliable workhorse processes in the VLSI technology. A schematic view in Fig. 3 below shows the various areas in a CMOS device process in which I/I plays an important role, mainly for the channel and contact formation, but also for the background doping level in the so-called wells.

The number of I/I steps in a state-of-the-art process is more than 20. The various different fluencies and energies needed are represented in Fig. 4.

Note that fluence is the SI unit corresponding to the number of ions impinging per unit area. In the semiconductor industry the standard terminology is "dose", which in other applications has the meaning of deposited energy per kg. The dose range is from 10^{11} to 10^{16} cm^{-2} for device fabrication, whereas higher doses are needed for some special applications such as SOI substrates; see Sect. 3.3 below. The I/I energy range is from several hundreds of eV for ultra shallow junctions to several MeV for retrograded wells; see Fig. 3. It can be inferred from this discussion that several dedicated tools are needed to cover this energy-dose space. The tools are normally grouped into low- and high-energy tools, respectively. The implantation current

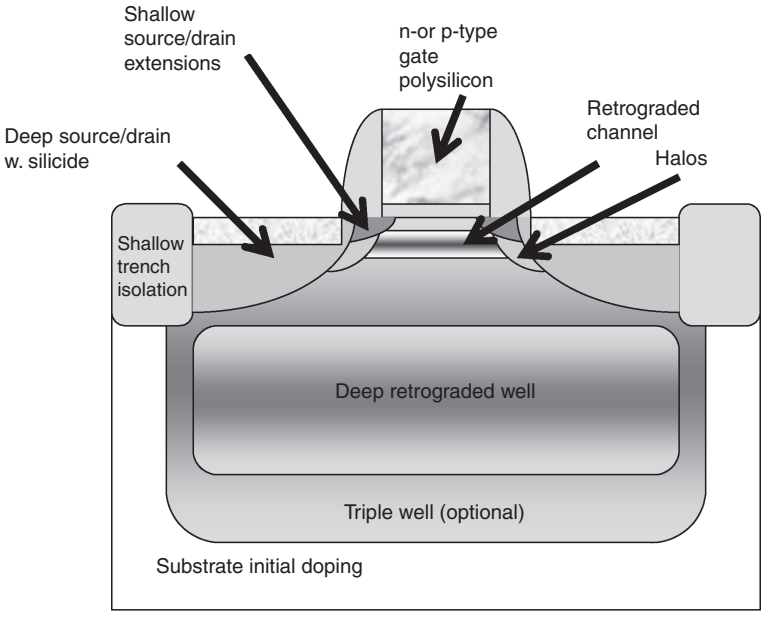

Fig. 3 Overview of the I/I steps needed to fabricate integrated circuits in CMOS technology

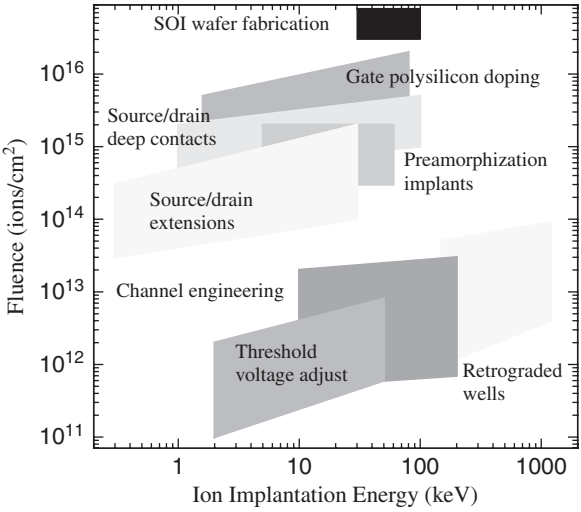

Fig. 4 Fluence-energy space of ion implantations for silicon device and process technology. Adapted after Doering and Nishi [12]

is the second important category; however in view of maximum wafer throughput, there is limited use for low current. Special configurations are used if angled implants (tilting) or wafer rotation is needed. Single wafer tools are predominant in the industry because of uniformity constraints.

In this context, it should be mentioned that CMOS uses two type of transistors, n-channel and p-channel field effect transistors (FETs). The basic building block in a circuit is the inverter, consisting of one pFET and one nFET. To form pFETs and nFETs in the same substrate, separate regions of opposite doping polarity are needed. For the n-type doping As is preferred because of its slower diffusion compared to P; an exception to this rule is of course deep diffusions or buried layers. For the p-type doping B is the only candidate with high enough solubility and hence enough active dopants. To control the depth of the profile, molecular ions or clusters such as BF_2 and $B_{10}H_{14}$ can be used. However, BF_2 has a disadvantage, in that the presence of fluorine counteracts high activation of B. The p-type and n-type substrate regions are achieved by high energy I/I of wells, sometimes called tubs. By using high energy implantation the peak of the well profile can be positioned without long thermal diffusion of dopants; this gives a good control over lateral dimensions, and the device-device separation and footprint can be reduced. A so-called retrograde profile, in which the peak is located at the bottom of the well, is desired to suppress so-called latch up, which is an undesired leakage path between n-well and p-well. The commonly used structures today are referred to as twin well or triple well, of which the latter provides independent body biasing and suppressed substrate noise in mixed signal applications. Well formation is normally self-aligned to the already formed oxide-filled shallow trench isolation (STI).

Doping of the channel region requires several implantations of varying energy and dose. Each has its specific purpose, namely punch through stopper, retrograde channel implant, and threshold voltage (V_T) adjust. See Fig. 5 for typical depth

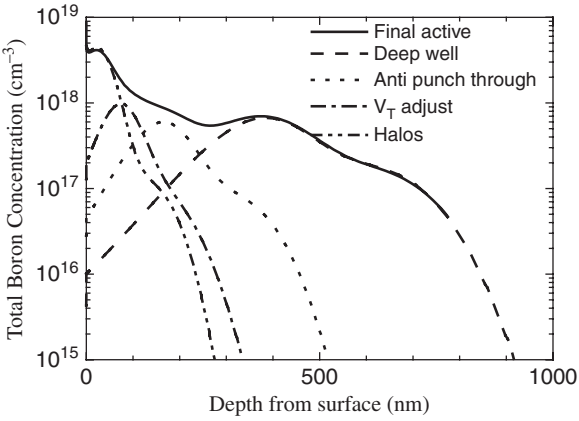

Fig. 5 Typical doping depth profile in the channel and well regions of a 50 nm gate length MOSFET, based on simulation data

profiles, including the retrograde p-well. The dose variation control of the V_T adjust is critical for device and circuit applications.

The source and drain regions are formed in a self-aligned manner, after the patterning of the gate electrode. The source/drain implantations include a deep contact region with low sheet- and contact-resistance and a shallow region, which is called the extension. Sidewall spacers are used to offset the deep region from the intrinsic transistor channel.

At this step in the process sequence, the dual doping of the polysilicon gates is also introduced by masked ion implantations.

High activation and shallow junctions are needed to optimize short channel effects and to minimize the junction capacitance. These are two competing requirements, and they are intimately coupled by the point defect creation and diffusion. Implant energies of 1 keV or less are used for the B-profiles in the pFETs.

As the implant energies are reduced further, it becomes difficult to create an ion beam with high enough current density and energy purity. A future potential technique for the purpose of low energy, high current implantation is the plasma immersion ion implantation technology. This technique was researched heavily during the early 1990s and successful demonstrations have been published recently [13–15]. Commercial applications have been found in highly doped polysilicon for memory applications.

Halo implants, as shown in Fig. 6, can be used to counterdope the extensions and hence make them even more abrupt [16]. The halo implantations are normally performed with a tilt of 30–60°. Using a tilt puts some of the halo dose in the channel, and hence V_T is affected. Especially for short channel devices, the halos or pockets are present everywhere in the channels, i.e., the profiles from the source and drain side, respectively, will merge. This gives rise to a phenomenon known as reverse short channel effect. Tilted implantations of 7° are commonly used to avoid boron channelling in preferred crystal directions.

Alternative techniques for the activation anneal such as spike or laser annealing should be considered. Spike annealing takes advantage of the different time con-

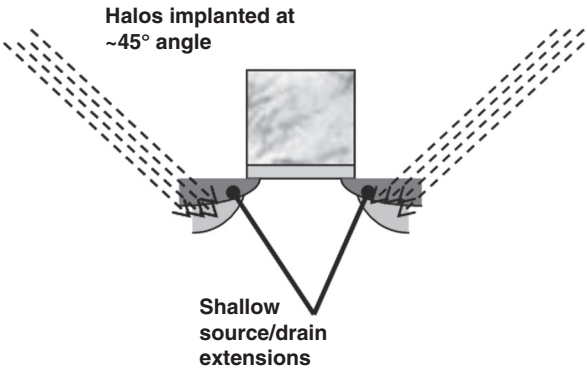

Fig. 6 Example of tilted ion implantation to form the so-called HALO regions to prevent short channel degradation in ultra-scaled MOSFETs

stants involved in defect and dopant diffusion, and laser annealing causes a local recrystallization of the doped region. Activation of shallow junctions can be further improved by *pre-amorphization* using Ge ion implantation or *co-implantation* using C or F [17–20] with different dopant species, especially B. Both these methods affect the end of range implantation defect profiles and hence give additional control of the final resulting active profile.

3 Performance Boosters in CMOS Technology

The need for ever higher device performance is very challenging. In fact, the need for better materials properties has led to an increased effort in materials technology. In this section both substrate material engineering and new material choices will be discussed.

3.1 High-κ/Metal Gate

From the 45 nm node the standard SiO_2 gate dielectric cannot fulfil the requirements in the roadmap. This is especially important for low-power operation, and high-κ/metal gate has not yet been optimized for high-speed devices. The first announcement from the industry of products incorporating high-κ/metal gate was made in 2007, shortly before the ITRS roadmap prediction. These devices use hafnium Hf-based stacks, including well controlled interfaces to both silicon channel and gate electrode. In fact, the industry standard polysilicon gate technology is not compatible with Hf-based films unless intermediate layers are used.

From a fundamental device physics view, several candidate materials have been studied and Hf offers a medium κ-value in combination with suitable conduction and valence band offsets for low direct leakage. For ultimate technology scaling, other rare earth metals must be considered, such as lanthanum, La [21–23].

Ion beam techniques have found wide use in the structural analysis of high-k materials. In chapter “Low and Medium Energy Ion Scattering for Near Surface

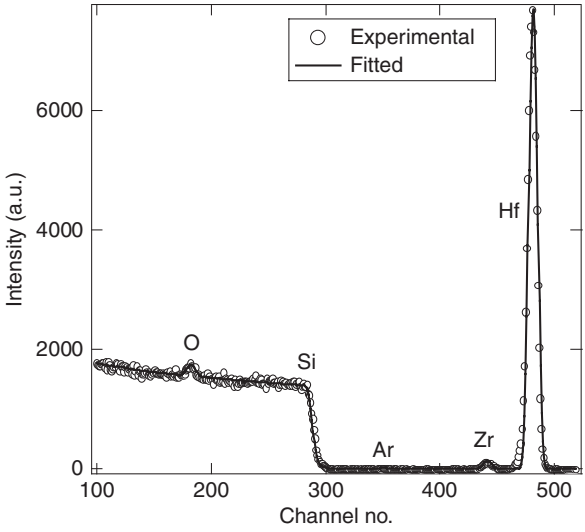

Fig. 7 RBS analysis of 30 nm high-k film to determine (stoichiometric) composition. Hf : O = 1 : 2.08, Zr: 1.5%, Ar: 1%

Structure and Nanoscale Depth Profiling" *medium energy ion scattering* and *time of flight-energy elastic recoil detection analysis* (ToF-E ERDA) will be discussed. Another commonly used technique is *Rutherford Back Scattering* (RBS). RBS is an important analysis tool for thin films in microelectronics. The compositon of Hf-based films can be determined with resolution below the percent level; an example is shown in Fig. 7 [24].

3.2 Substrate Engineering

Improved performance of standard CMOS technology is possible by replacing the bulk silicon wafer with another starting material. Two types of substrates will be discussed, silicon-on-insulator (SOI) and strained virtual substrates (VS). The two main advantages of SOI are reduced junction-substrate leakage, and hence low power operation; and better control of the short-channel effects, since the buried oxide layer prevents the drain side electric field from reaching the source. Using VS technology the fundamental properties of silicon, mainly carrier mobility, can be improved. A more unconventional solution would be to use high mobility III-V material in the channel region. This is currently a subject of ongoing research and will be mentioned below.

3.3 SOI

SOI was originally intended for low-power logic and also used for a long time in radiation-hard circuits. However, at the 0.18 μm CMOS technology node,

SOI was introduced in microprocessors by some companies to increase the performance/speed.

Ultrathin body SOI is one of the technologies on the roadmap beyond the current 45 nm node. However, the introduction of ultrathin body SOI has been pushed back to later nodes, because of innovations in other areas.

In this section we will discuss the fabrication of high quality SOI substrates using the most common techniques, namely separation by implantation of oxygen (SIMOX) and Smartcut®/Unibond®. Ion implantation is one of the key technologies to realize this type of substrate. Also needed are wafer bonding and planarization. In SIMOX wafers, a buried oxide layer is formed by a high dose (fluence) ($1 \times 10^{18}\,\mathrm{cm}^{-2}$) followed by a high temperature (1320°C) anneal. For reasonable throughput, high current implanters must be used with a beam current of 100 mA. This is beyond the capability of standard implanters. On the other hand, SmartCut® relies on hydrogen implantation of an oxidized wafer to a dose (fluence) of about $5 \times 10^{16}\,\mathrm{cm}^{-2}$; cf. Fig. 4 above. A schematic process flow is illustrated in Fig. 8. The implanted hydrogen creates local voids or microcavities in the wafer used as starting material. This wafer is then bonded to another oxidized handle wafer and annealed at 600°C to produce a cut (at the peak of the hydrogen profile). The result becomes one SOI wafer with a thin, device-grade, silicon top layer, and one handle wafer for reuse.

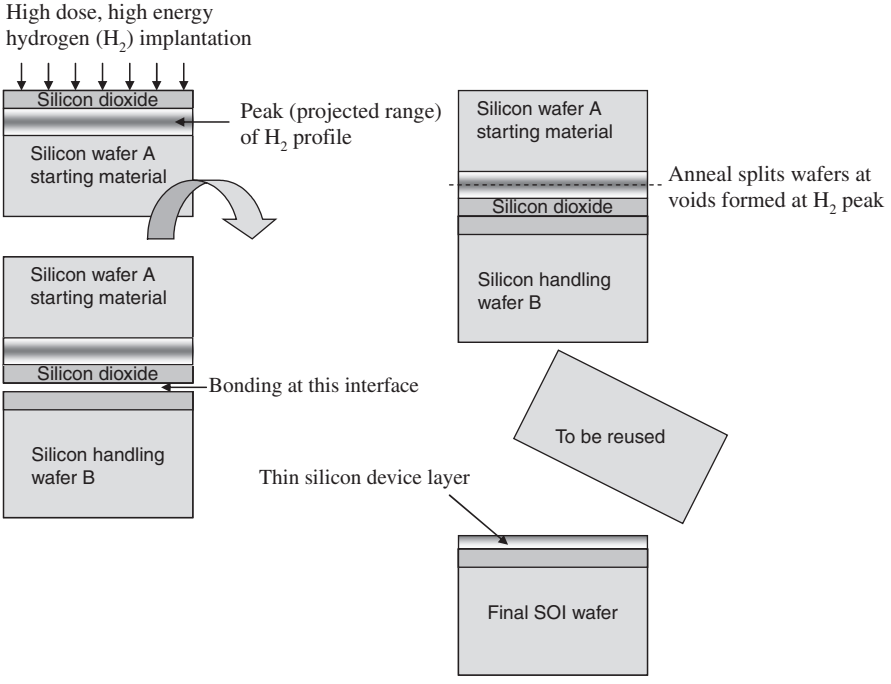

Fig. 8 Example of hydrogen implantation to form an SOI substrate with a buried oxide layer [16, 25]

3.4 Virtual Substrates

Although silicon has many desirable properties for integrated circuit manufacturing, the intrinsic carrier mobility for both electrons and holes is comparatively low. A strained silicon layer can be utilized to significantly increase the mobility in the MOSFET channel. One way to accomplish this is the use of biaxially strained virtual substrates (VS). The other approach is locally induced uniaxial strain, using dielectric films as stressors. In VS technology, strain is introduced by gradually changing the lattice constant by introducing high concentrations of Ge. Typically 1% of Ge is added per micrometer, until a final concentration of 20–30% is reached, e.g., a composition of $Si_{0.8}Ge_{0.2}$. This constitutes the SiGe relaxed buffer layer. On top of this layer a thin silicon layer is grown. The lattice mismatch between the silicon and the relaxed $Si_{1-x}Ge_x$ results in a tensile strain in the thin silicon films, since Ge has a larger lattice constant. A high resolution TEM image of a VS substrate is shown in Fig. 9.

3.5 Heteroepitaxy

What will be the technology roadmap after 2015? The European technology platform ENIAC has depicted the scenario in their recently published Strategic Research Agenda [26]. The main scenario in the agenda is still based on a silicon platform; however, some add-on solutions are pointing to the introduction of III–V technology on silicon.

Concerning enhanced speed, many options are already approaching enough maturity to be applied in commercial technology. Examples include inducing stress in the conductive channel of the transistor and/or using different crystal orientations. In a longer term scenario, increased speed may be achieved by replacing silicon channels with more conductive materials such as germanium (Ge) or III-V

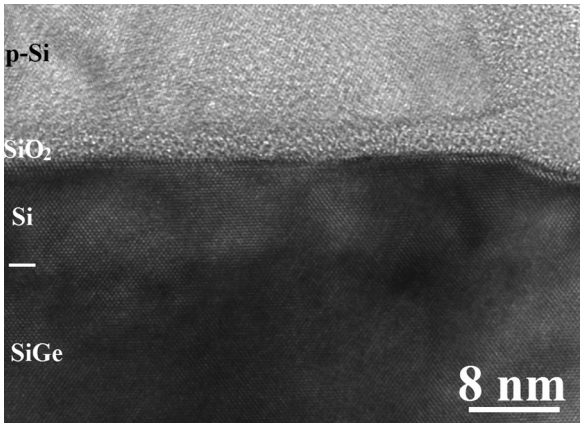

Fig. 9 High resolution transmission electron microscope (TEM) image (with near atomic resolution) of a complete MOSFET device structure on a virtual substrate. The labels indicate the gate oxide (SiO_2), polysilicon gate electrode (p-Si), strained channel layer (Si), and relaxed SiGe buffer layer

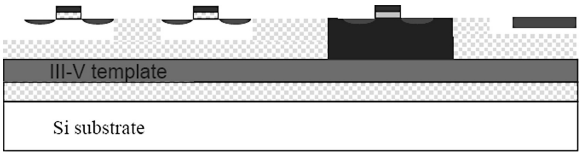

Fig. 10 Cross section of a future silicon wafer with integrated areas of III-V devices. Courtesy of E. Fitzgerald, Massachusetts Institute of Technology, Cambridge

compounds embedded in more sophisticated architectures (e.g., germanium-on-insulator I, III–V on germanium, and nanowires) [26].

By using lattice matching, other high mobility materials such as GaAs [27, 28] and InSb [29] compounds can be used in the channel of a field effect transistor. Excellent results have been achieved with zero antiphase boundary GaAs grown on Si. Introducing a clever materials platform called SOLES (silicon on lattice engineered substrates) MIT researchers have shown that this integration technique also is manufacturable. The concept is schematically illustrated in Fig. 10, in which a buried III-V template layer allows growth in selected device regions, while silicon is available on the remaining part of the wafer surface to form more conventional devices.

4 Lithography

In this section we review current trends in lithography for CMOS integrated circuit applications. The patterning of the small features in integrated circuits is one of the increasingly difficult challenges as the minimum pitch as well as the isolated feature size continue to shrink with scaling. The feature size is now considerably smaller than the optical wavelength used in lithography. In fact, standard DUV lithography with a 193 nm light source is used for the 45 nm CMOS technology node in which the patterned gate length is even smaller—about 30 nm.

This has been made possible because of different kinds of improvements of the lithographic process, such as phase shifting masks (PSM) and optical proximity correction (OPC). However, the underlying principle is a detailed modelling of the electromagnetic wave propagation in the optical projection system, including lenses and the reticle itself. In this way the reticle can be corrected to produce the desired shape of the printed feature on the wafer. A common measure of the lithographic capability is the area of the very dense 6T-SRAM memory cell, which today occupies less than $0.3\,\mu m^2$.

As the use of the 193 nm tools reaches its limitation, one important technology change is to introduce a medium with higher refractive index in the optical path. Immersion in water can increase the numerical aperture (NA) of the lenses, and smaller patterns can be resolved. In practice, this means that a thin layer of water is placed between the optical projection column and the resist coated wafer surface.

Much effort is also placed on light sources with shorter wavelength, so-called extreme ultraviolet (EUV). This will be accompanied by a change in the optics which will be reflective (using mirrors) instead of refractive (lenses). Masks which are transparent to these wavelengths are also needed.

The alternatives to optical lithography using reticles are based on direct-writing techniques, in which an electron beam is widely used for nanostructures and for special applications, such as dense optical gratings. Focused ion beam (FIB) systems have also been proposed. For an extensive treatment of FIB, refer to chapter "Focused Ion Beam Machining and Deposition". Typically, ions such as Ga^+ (atomic mass 31) are used. For FIB lithography, lighter ions such as protons (H^+) may be used; for more details see chapter "Proton Beam Writing: A New 3D Nano Lithographic Technique". Some of the issues here are wafer throughput and line edge roughness due to electron/ion scattering. Electron beam systems are widely used for lithographic reticle (mask) manufacturing. FIB is used for mask repair and also for postprocessing analysis and correction of failures in integrated circuits.

Finally, we briefly discuss a technique called sidewall transfer (spacer) lithography, in which a combination of optical lithography and selective directional etching is used [30]. This technique has superior control of line edge and line width roughness compared to, e.g., electron beams. The basic principle is to create a thin sidewall inside an etched opening in a patterned support layer. The patterning of the support layer is done by optical lithography. The support layer in then removed, by selective etching, and the sidewall will now serve as a hard mask for the actual 'device pattern,' e.g., a polysilicon gate line, as shown in Fig. 11.

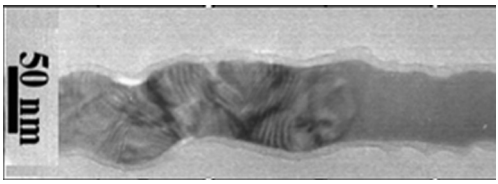

Fig. 11 Example of a 50 nm polysilicon gate patterned by sidewall transfer lithography, showing the effect of line width and line edge roughness (LWR/LER)

5 Conclusions

This chapter has discussed the background, present technology concerns, and short future outlook for nanoelectronic semiconductor technology. We have addressed the immense importance of the technology from a socioeconomic perspective and shown that rapid progress continues with unbroken strength. We have also discussed selected technology solutions and commented on the importance of ion implantation technologies in this field. Finally, a brief outlook on new substrate and materials requirements was given, and an alternative based on heterogeneous materials integration was shown.

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