

Porous Silicon in Practice

Preparation, Characterization and Applications

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1

Fundamentals of Porous Silicon Preparation

1.1 Introduction

Porous silicon was accidentally discovered by the Uhlirs, a husband and wife team working at Bell Laboratories in the mid 1950s. They were trying to develop an electrochemical method to machine silicon wafers for use in microelectronic circuits. Under the appropriate electrochemical conditions, the silicon wafer did not dissolve uniformly as expected, but instead fine holes appeared, propagating primarily in the $\langle 100 \rangle$ direction in the wafer. Since this did not provide the smooth polish desired, the curious result was reported in a Bell labs technical note [1], and then the material was more or less forgotten. In the 1970s and 1980s a significant level of interest arose because the high surface area of porous silicon was found to be useful as a model of the crystalline silicon surface in spectroscopic studies [2–5], as a precursor to generate thick oxide layers on silicon, and as a dielectric layer in capacitance-based chemical sensors [6].

Interest in porous silicon, and in particular in its nanostructure, exploded in the early 1990s when Ulrich Goesele at Duke University identified quantum confinement effects in the absorption spectrum of porous silicon, and almost simultaneously Leigh Canham at the Defense Research Agency in England reported efficient, bright red–orange photoluminescence from the material [7, 8]. The quantum confinement effects arise when the pores become extensive enough to overlap with each other, generating nanometer-scale silicon filaments. As expected from the quantum confinement relationship [9], the red to green color of photoluminescence occurs at energies that are significantly larger than the bandgap energy of bulk silicon (1.1 eV, in the near-infrared).

With the discovery of efficient visible light emission from porous silicon came a flood of work focused on creating silicon-based optoelectronic switches, displays, and lasers. Problems with the material's chemical and mechanical stability, and its disappointingly low electroluminescence efficiency led to a waning of interest by the mid 1990s. In the same time period, the unique features of the material—large surface area, controllable pore

sizes, convenient surface chemistry, and compatibility with conventional silicon microfabrication technologies—inspired research into applications far outside optoelectronics. Many of the fundamental chemical stability problems have been overcome as the chemistry of the material has matured, and various biomedical [10–18] sensor, optics, and electronics applications have emerged [10].

Porous silicon is generated by etching crystalline silicon in aqueous or non-aqueous electrolytes containing hydrofluoric acid (HF). This book describes basic electrochemical and chemical etching experiments that can be used to make the main types and structures of porous silicon. Beginning with measurement of wafer resistivity, the experiments are intended for the newcomer to the field, written in the form of detailed procedures, including sources for the materials and equipment. Experiments describing methods for characterization and key chemical modification reactions are also provided. The present chapter gives an overview of fundamentals that are a useful starting point to understand the theory underlying the experiments in the later chapters.

1.2

Chemical Reactions Governing the Dissolution of Silicon

The formation of porous silicon involves reactions of Si–Si, Si–H, Si–O, and Si–F bonds at the surface of the silicon crystal. The relative strengths of these bonds, obtained from thermodynamic measurements of molecular analogues, are given in Table 1.1. While one might think that the strengths of these bonds would determine the relative stability of each species on a silicon surface, the electronegativity of the elements plays a much more important role. Si–H and Si–C species tend to passivate the silicon surface in aqueous solutions, while the Si–F bond is highly reactive. Electronegative elements such as O and F form more polar Si–X bonds, making the silicon

Table 1.1 Enthalpies of some Si–X bonds.

| Compound | Bond | Enthalpy, kcal mol ⁻¹ |
|--------------------------------------|-------|----------------------------------|
| Me ₃ Si–SiMe ₃ | Si–Si | 79 |
| Me ₃ Si–CH ₃ | Si–C | 94 |
| Me ₃ Si–H | Si–H | 95 |
| Me ₃ Si–OMe ₃ | Si–O | 123 |
| Me ₃ Si–F | Si–F | 158 |

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atom susceptible to nucleophilic attack. The surface of freshly prepared porous silicon is covered with a passivating layer of Si–H bonds, with minor quantities of Si–F and Si–O species.

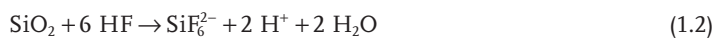
1.2.1

Silicon Oxides and Their Dissolution in HF

Silicon is thermodynamically unstable in air or water, and it reacts spontaneously to form an oxide layer. The oxide can be nonstoichiometric and hydrated to various degrees, though the simple empirical formula is silicon dioxide, SiO₂ (Equation 1.1). SiO₂ is a key thermodynamic sink in the silicon system.



SiO₂ is an electrical insulator that forms passivating films on crystalline silicon; preparation of porous silicon thus requires an additive in the solution to dissolve the oxide and allow electrochemical oxidation to continue. The Si–F bond is the only bond stronger than Si–O, and it is the Si–F bond enthalpy that drives the main chemical dissolution reaction used to make porous silicon. In the presence of aqueous HF, SiO₂ spontaneously dissolves as SiF₆²⁻ (Equation 1.2).



The reaction of SiO₂ with HF is a common industrial reaction. It is used to prepare frosted glass from plate glass and to remove SiO₂ masking layers in the processing of silicon wafers in microelectronics. The silicon hexafluoride ion (SiF₆²⁻) is a stable dianion that is highly soluble in water. Thus fluoride is the most important additive used in the preparation of porous silicon, dissolving the insulating oxide that would otherwise shut down the electrochemical corrosion reaction.

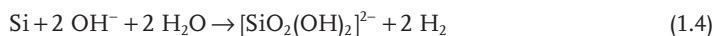
1.2.2

Silicon Oxides and Their Dissolution in Basic Media

In the absence of fluoride ion, SiO₂ on the surface of a silicon wafer protects the underlying silicon from further oxidation. While this is true in acidic or neutral aqueous solutions, in basic solutions hydroxide ions attack and dissolve the oxide by Equation 1.3:



The net dissolution reaction for silicon in basic media then becomes:



The reaction represented by Equation 1.3 is highly simplified. The species $[\text{SiO}_2(\text{OH})_2]^{2-}$, the doubly protonated form of silicic acid, is only one of many water-soluble forms of silicon oxide. The fundamental oxide-containing unit is the SiO_4^{4-} tetrahedron, known as the orthosilicate ion [11]. Orthosilicate itself is highly basic, and in aqueous solutions it is never present as the naked SiO_4^{4-} ion. The fully protonated species is orthosilicic acid, $\text{Si}(\text{OH})_4$, and this is the generic formula that is often presented in the literature to indicate all the water-soluble forms of silicic acid. The first ionization constant ($\text{p}K_a$) of $\text{Si}(\text{OH})_4$ is about 10, and the second ($\text{p}K_a$) is around 12. Thus the $[\text{SiO}_2(\text{OH})_2]^{2-}$ ion depicted in Equation 1.3 is only present in highly basic ($\text{pH} > 12$) solutions. In neutral or acidic solutions, $\text{Si}(\text{OH})_4$ is the predominant monomeric form.

When the solution concentration of $\text{Si}(\text{OH})_4$ is sufficiently large, silicic acid condenses into oligomers. Various “polysilicic acids” with the general formula $[\text{SiO}_x(\text{OH})_{4-2x}]_n$, where $2 > x > 0$, are present in solution [11]. In neutral or acidic solutions these oligomers can condense to the point of precipitation, essentially the reverse of Equation 1.3:



The reaction represented in Equation 1.5 is the key reaction in the “sol–gel” process, often used to prepare colloids, films, or monoliths of porous silica from solution precursors [12]. The insolubility of SiO_2 in acidic solutions explains why elemental silicon does not corrode appreciably at $\text{pH} < 7$; the oxide provides a protective, passivating layer. The same is not true in basic solutions; here the solubility of silicon oxide drives silicon oxidation and dissolution by Equation 1.4. The high surface area and relatively strained nature of Si–Si bonds in porous silicon make the reaction with hydroxide ion quite rapid. In Chapter 2 we will employ this reaction (using aqueous KOH) to dissolve a porous silicon layer in order to determine its porosity. The Si–Si bonding in bulk silicon is less strained, and bulk silicon dissolves more slowly in basic solutions. In these and other situations where the oxide is soluble, dissolution of silicon becomes limited by surface Si–H species.

1.2.3

Silicon Hydrides

The reaction of silicon with water should be analogous to the reaction of metallic sodium in water; elemental silicon is electropositive enough to spontaneously liberate hydrogen from water. However, silicon does not dissolve in acidic solutions, even if the solution contains fluoride ion to remove the passivating SiO_2 layer. Although thermodynamically feasible, dissolution of silicon in aqueous HF is slow unless strong oxidizing agents (such as O_2 or NO_3^-) are present in the solution, or unless the oxidation reaction is driven by electrochemistry. The reason is that corrosion becomes kinetically limited by the passivating nature of surface hydrides.

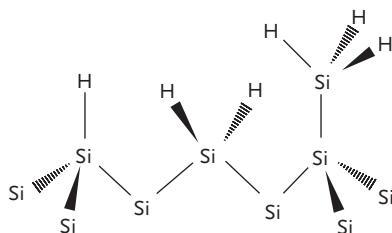


Figure 1.1

Hydrides on the porous silicon surface.

The freshly etched surface of porous silicon is terminated primarily with hydride species. Residual oxides or

fluorides are removed by the HF

electrolyte. Three types of surface hydrides are depicted: SiH, SiH₂, and SiH₃.

When silicon is chemically or electrochemically etched in HF-containing solutions, the exposed silicon surface becomes terminated with H atoms (Figure 1.1). The mechanism of this reaction is described in more detail later in this chapter. The surface Si–H species are not readily removed by acid, and they must be oxidized to allow the silicon corrosion reaction to continue. In alkaline solutions, OH[−] is able to attack these species because it is a good nucleophile. Nucleophilic attack is an important reaction in the silicon system, and it is discussed in more detail in Chapter 6. The Si–H species on porous silicon can also be removed by the action of a cationic surfactant, which polarizes the surface and induces nucleophilic attack by water, even in acidic solutions [13]. This reaction is also discussed in Chapter 6.

1.3

Experimental Set-up and Terminology for Electrochemical Etching of Porous Silicon

In an electrochemical reaction, two electrodes are needed. One supplies electrons to the solution (the cathode) and the other removes electrons from the solution (the anode). It is important to keep in mind that the two electrodes are required to maintain charge neutrality and to complete the electrical circuit. Regardless of the oxidation or reduction reactions occurring at the electrodes, you cannot perform electrochemistry if you do not complete the circuit. This means that at least two reactions are occurring simultaneously in an electrochemical cell, the anode (oxidation) reaction and the cathode (reduction) reaction. Electrochemists refer to these as “half-reactions.” A schematic of a two-electrode cell for etching silicon, with the relevant half-reactions, is shown in Figure 1.2.

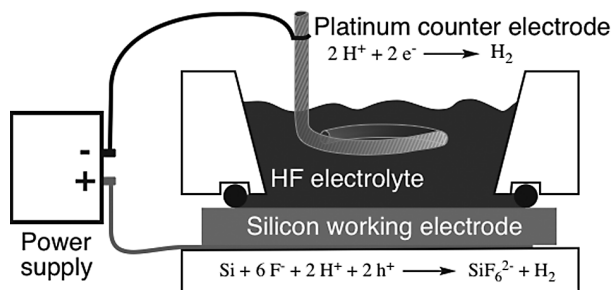


Figure 1.2

Schematic of a two-electrode electrochemical cell used to make porous silicon. Silicon is the working electrode. The working electrode is an anode in this case, because an oxidation reaction

occurs at its surface. The cathode counter-electrode is typically platinum. The main oxidation and reduction half-reactions occurring during the formation of porous silicon are given.

1.3.1

Two-Electrode Cell

In the two-electrode cell, electrochemical reactions must occur at both electrodes, but generally you are interested in the reaction at only one of these. In the case of porous silicon formation, the silicon electrode is the important one. It is the anode, and the chemical being oxidized is the silicon itself. The cathode used in porous silicon etching cells is usually platinum, and it is separated from the silicon electrode by a few mm to several cm of electrolyte solution, or in some cases by a membrane or salt bridge. The electrochemical reaction occurring at the platinum electrode is primarily the reduction of protons to hydrogen gas. Electrochemists refer to the silicon electrode as the “working electrode”, and the platinum electrode as the “counter-electrode” in this experiment. We are generally not concerned with the counter-electrode (cathode) reaction, although it can produce byproducts that interfere with the silicon electrocorrosion reaction or otherwise limit the silicon etching process. The design of electrochemical cells and practical considerations regarding the counter-electrode and other cell materials are discussed in Chapter 2.

1.3.2

Three-Electrode Cell

A three-electrode electrochemical cell is used when one wants to measure both the current and the potential of an electrochemical reaction simultaneously [14]. This situation is commonly encountered in electrochemistry,

because it allows the identification of the driving force of an electrochemical process. In a three-electrode configuration, a high-impedance reference electrode is connected into a specialized feedback circuit. The reference electrode is designed to precisely control the electrochemical processes that can occur at its surface, so that the electrochemical potential is well defined and does not drift. A common reference electrode used in aqueous systems is the saturated calomel electrode. It is defined by the half-reaction of mercury metal (Hg) with mercury (I) chloride (Hg_2Cl_2) in a solution saturated with potassium chloride (KCl). The mercury, mercury (I) chloride, and potassium chloride are all contained in a small tube separated from the electrochemical cell by a porous glass membrane (typically Vycor glass). The presence of the membrane and the high impedance (resistance to current flow) established by the measurement circuitry ensure that only a small ion current is allowed to flow between the reference electrode compartment and the rest of the electrochemical cell, maintaining a stable reference potential. This sort of cell is not compatible with solutions containing HF, and so various other reference electrode configurations have been used for porous silicon experiments.

A common reference electrode for HF systems is a bare platinum wire placed in a solution of HF, separated from the main electrochemical compartment by a thin plastic capillary tube. This is not a particularly reproducible reference electrode, since the electrochemical reaction potentials are sensitive to surface impurities on the Pt wire. Nevertheless, the electrode potential is fairly stable over periods of hours, and it is common practice to use such electrodes, referred to as “pseudo-reference” electrodes to indicate their tenuous relationship to true thermodynamic potentials. Throughout this book we are less concerned with the potential at the silicon surface and more concerned with the total current flowing through it. This is because most of the key properties of a porous silicon film: the porosity, pore size, and thickness are determined by the current. A two-electrode configuration is sufficient to set this parameter, and it is used in the experiments described in this book.

1.4 Electrochemical Reactions in the Silicon System

A representative current–potential curve for silicon in an HF electrolyte is shown in Figure 1.3. The curve displays characteristics common to the Si/HF system: an initial exponential rise in current with applied potential that reaches a maximum, decreases somewhat, and then increases more slowly at increasingly positive potentials. There are three regions usually defined: the porous Si formation region, a transition region, and the electropolishing regime.

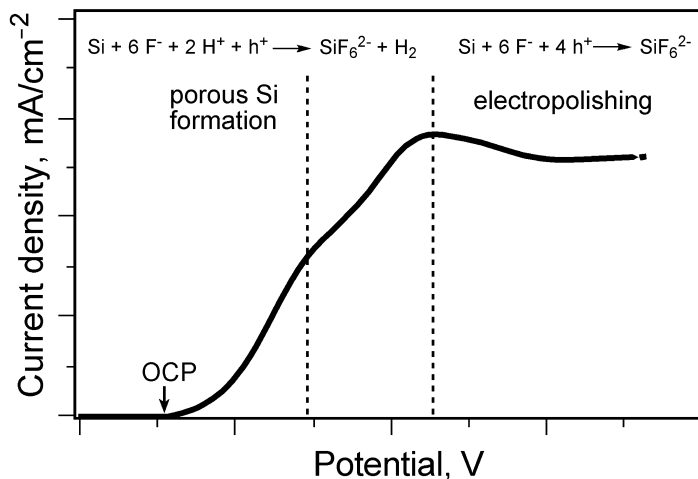


Figure 1.3

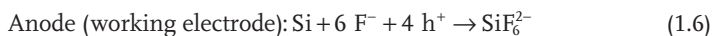
General current density versus applied potential curve for electrochemical etch of silicon in an HF electrolyte, showing the regimes for porous silicon formation and for electropolishing. The relevant 2-electron and 4- electron oxidation

open circuit potential, or rest potential, of the silicon electrode. Data for this curve correspond to a moderately doped p-type silicon wafer in 1% HF solution, adopted from Zhang, X. G. Morphology and Formation Mechanisms of Porous Silicon. *J. Electrochem. Soc.* 151, C69–C80 (2004).

1.4.1

Four-Electron Electrochemical Oxidation of Silicon

To drive the corrosion of silicon electrochemically, positive current must be passed through the silicon electrode. The simplest reaction that can be expected during anodic dissolution of silicon in fluoride-containing solutions is the 4-electron oxidation represented by Equation 1.6. Here we use holes in the silicon valence band as the oxidizing equivalents. Note this equation is written as a half-reaction. As mentioned above, the electrons supplied by silicon at the working electrode must be balanced by a reduction half-reaction that consumes electrons at the counter-electrode. The electrochemical process performed by these electrons is usually the reduction of water to hydrogen gas.



It turns out that the 4-electron half-reaction represented by Equation 1.6, the anodic oxidation of silicon, is the predominant reaction when the electrocorrosion reaction is running at “full speed,” and no porous silicon is

being formed. This condition is referred to as electropolishing, and it occurs at the more positive electrode potentials depicted in Figure 1.3. It should be noted that this is an idealized equation, and that other compounds are involved in the silicon-HF system during electrocorrosion. For example, SiF_2 , SiF_4 , and the various members of the $\text{SiH}_n\text{F}_{(4-n)}$ family are thermodynamically accessible, though they are generally minor byproducts in the reaction. The active fluoride-containing species in aqueous and non-aqueous HF solutions include HF, $(\text{HF})_2$, and HF_2^- .

1.4.2

Two-Electron Electrochemical Oxidation of Silicon

When the Uhlirs first prepared porous silicon, they noted bubbles rising from the silicon wafer (Figure 1.4) [1]. They assumed this gas was oxygen. For a “normal” aqueous electrochemical process, splitting of water is an often-encountered side reaction—especially if the applied potential exceeds the thermodynamic water splitting potential of 1.23 V and the electron transfer kinetics of the reaction of interest are sluggish. In the electrolysis

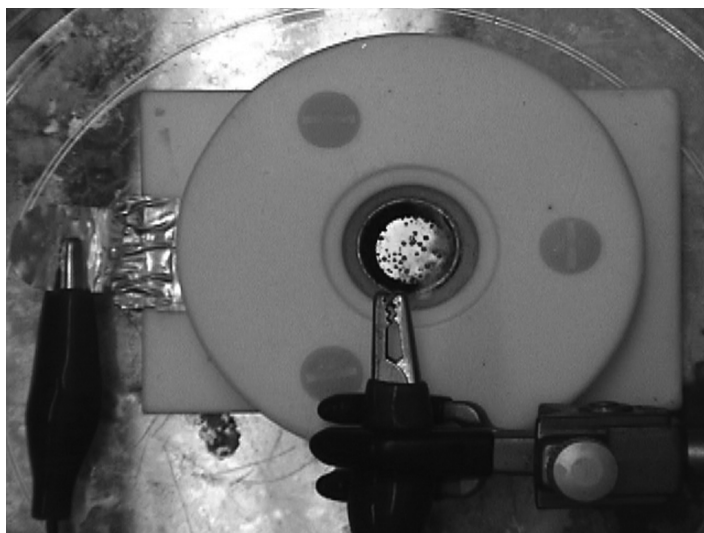


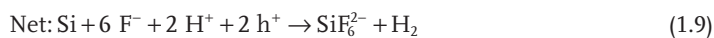
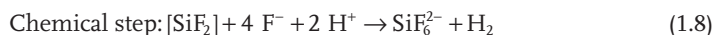
Figure 1.4

Electrochemical etching of silicon in the current regime where porous silicon is formed. This is a top view of an

electrochemical etching cell. Bubbles of hydrogen gas are observed forming at the silicon surface.

of water, hydrogen gas is expected to form at the cathode (platinum wire in our case) and oxygen gas should form at the anode (the silicon wafer). The bubbles rising from the platinum counter-electrode (cathode) are indeed hydrogen, coming from the water electrolysis reaction. When the Uhlirs collected the gas coming from the silicon electrode, they expected it was oxygen and performed the classical glowing wooden splint experiment: placing the burning embers of a wooden stick into pure oxygen causes the stick to catch fire. Instead of a flame, they observed a small but startling explosion—the gas they had collected was hydrogen.

The unexpected evolution of hydrogen during the electrocorrosion of silicon is related to the fact that spontaneous reduction of water by silicon is thermodynamically favored. The kinetics of this reaction are slow for silicon in its elemental form (oxidation state 0), but silicon in its +2 oxidation state reacts rapidly with water, liberating hydrogen and producing silicon in its most common +4 oxidation state. The 2-electron oxidation process is represented in the two-step formalism of Equations 1.7 and 1.8. As in Equation 1.6, we use holes in the silicon valence band as the oxidizing equivalents. Note the lower case h^+ depicts a valence band hole and the upper case H^+ is a proton in these equations.



The two-electron process of Equation 1.9 predominates at lower applied potentials, and it is the main half-reaction responsible for porous silicon formation. The region of the current density–potential plot in Figure 1.3 labeled “PS formation” corresponds to this regime.

1.4.3

Electropolishing

When the current–potential relationship is in the electropolishing regime, silicon atoms are removed isotropically (i.e., no pores form). The net result is that the silicon wafer becomes thinner. This was the goal that the Uhlirs were pursuing in the mid 1950s when they accidentally discovered porous silicon. Electropolishing usually follows the 4-electron dissolution stoichiometry of Equation 1.6. Although some roughening can occur, electropolishing generally removes silicon atoms uniformly, and a smooth, polished surface will result if a polished wafer is used at the outset. An electropolishing reaction can be used to remove a pre-formed porous silicon layer from the silicon substrate (a “lift-off,” see Experiment 4.1). In this case the electropolishing reaction occurs at the porous silicon/crystalline silicon interface, undercutting the porous layer.

1.5

Density, Porosity, and Pore Size Definitions

Porous materials are less dense than the constituent materials from which they are made because they contain voids. These voids can be open to the outside world or closed off from it. The IUPAC recommendations for classifying porous media include definitions of density to account for the open or closed nature of the pores [15]:

Density:

true density: density of the material excluding pores and voids

bulk density: density of the material including pores, voids, and closed and inaccessible pores

apparent density: density of the material including closed and inaccessible pores

An illustrative example in the case of porous silicon: If we ignore the volume taken up by the surface hydrogen atoms, the “true density” of any porous silicon sample would be just the density of crystalline silicon found in the textbooks, 2.33 g ml^{-1} . To determine the “bulk density,” we need to know the geometry of our sample. Assume we use the Standard etch cell (Appendix 1), and etch a disc of porous silicon 1.2 cm in diameter (d) and $50 \mu\text{m}$ thick (L). The volume of the porous disc would be $\pi(d/2)^2L = 6.0 \times 10^{-3} \text{ cm}^3$, or 6 microliters. If the sample is 75% porous, the disc alone (removed from the silicon wafer) weighs 3.49 mg. The bulk density would be the mass of the sample divided by the volume it occupies, or $3.49 \times 10^{-3} / 6.0 \times 10^{-3} = 0.58 \text{ g ml}^{-1}$. Note that because the volume calculation includes the air in the voids, the bulk density is always smaller than the true density.

The value calculated for the apparent density is highly dependent on the method used to determine the volume of the sample. One common method to determine apparent volume is by liquid displacement. The sample is placed in a liquid of known volume, and the new volume is measured. The volume of the sample is just the difference in the two volumes. In this case, the fluid will only penetrate the pores that are accessible. In other words, the pores cannot be completely closed off, and they have to be large enough to accommodate the molecular dimensions of the liquid compound used. Thus the “apparent” density is as much a measure of the probe molecule as it is a measure of the sample.

The IUPAC defines porosity:

Porosity: ratio of the total pore volume V_p to the apparent volume V .

The meaning of the term “total pore volume” is dependent on the method. We must distinguish between “open porosity,” “closed porosity,” and “total porosity”:

Open porosity: the volume of pores accessible to a given probe molecule

Closed porosity: the volume of pores that are inaccessible to the probe molecule

Total porosity: open porosity + closed porosity; the volume of pores accessible to a given probe molecule plus the volume of pores that are inaccessible to the probe

Since it is prepared by corrosion of solid crystalline silicon, one can safely assume that all the pores in an as-formed porous silicon sample had to be accessible to the corrosion solution at the time of formation. It is, therefore, an open porous material with no inaccessible voids. However, if the material has been annealed, such that some of the pore mouths close off, the material will contain closed porosity. Also, because of the volume increase associated with conversion of Si to SiO₂, it is possible that a porous silicon sample will develop closed, inaccessible pores as it oxidizes. A similar situation could derive from chemical derivatization of the inner pore walls of a porous silicon sample, as we shall see in Chapter 6. Finally, it is important to keep in mind that the term “open porosity” is defined relative to a given probe molecule; a small pore that accommodates a molecule like ethanol may not accept a larger protein molecule. This is particularly true in biosensor and drug delivery applications, where the molecules of interest tend to be large.

We define three different pore size regimes, based again on the IUPAC “Recommendations for the characterization of porous solids:” [15]:

Micropores have widths smaller than 2 nm.

Mesopores have widths between 2 and 50 nm.

Macropores have widths larger than 50 nm.

The terms “nanoporous,” “nanopore,” and so on have come into vogue in recent years. It would be meaningless to follow the SI convention for the Greek prefixes, which would require that a nanopore be 1000 times smaller than a micropore—significantly smaller than the diameter of a hydrogen atom! While it currently carries no officially accepted definition, general usage indicates that a “nanomaterial” has structural features of the order of 100 nm or less. Thus the term nanoporous can be considered to be a general descriptor referring to any of the above macro-, meso-, or microporous materials with pore sizes less than 100 nm. In fact, this is more in line with the original Greek meaning of nano, which translates as “dwarf.”

Experiments 5.1 and 5.3 describe methods to measure porosity. Pore size can be measured by atomic force microscopy (AFM), high resolution scanning electron microscopy (SEM), or gas adsorption measurements. Measurement of adsorption isotherms of gases such as N₂ or CO₂ at low temperatures allows an indirect and widely accepted means of determination of pore size; the data are generally interpreted using models for gas adsorption, such as the BET, BJH, and BdB methods, which yield information on surface area and pore size, and a general idea of the shape of the pores. There are important assumptions related to pore shape and con-

nectivity used in these models, and acquisition and interpretation of such data are beyond the scope of this book. A general description of the methods are given in Chapter 5; for more details the reader should consult the relevant literature [16, 17].

The collection of cryogenic nitrogen adsorption isotherm data is one example of an experiment that determines pore size based on admission of a probe molecule. The experiment measures gas pressure in a chamber that contains the sample of interest and a known amount of nitrogen at a low temperature. The pore size can also be inferred from an optical reflectivity experiment that monitors the refractive index of a film upon exposure to probe molecules of various sizes. For example, the admission or exclusion of proteins based on size has been determined using this method [18–21].

1.6

Mechanisms of Electrochemical Dissolution and Pore Formation

The process controlling pore formation in porous silicon is a complicated mix of electronic and chemical factors, and it has been explored and discussed in detail [22]. The parameters of electrolyte composition, dopant type and concentration, applied voltage, temperature, and light intensity all play a role, and many competing mechanisms can be at play in a given experiment. However, there are some general shared features: (i) pores nucleate uniformly and with no particular order on the silicon surface, unless the wafer has been specifically pre-patterned; (ii) current flows preferentially near the pore bottoms; (iii) the pore walls become passivated, leading to dissolution of silicon primarily at the porous silicon/crystalline silicon substrate interface; (iv) once formed, the pores do not redistribute or reconstruct; and (v) all samples contain a distribution of pore diameters rather than a single pore size.

A wide range of pore diameters are accessible in the porous Si electrochemical system [23]. A dramatic example is shown in Figure 1.5, where the pore morphologies generated from n-type (phosphorus-doped) and highly doped p-type (boron-doped) silicon are compared. Both of those samples were generated using identical etching conditions (electrolyte, current density, and etch duration). The morphology of porous silicon derived from n-type wafers tends to consist of macropores, highly doped p+, p++, or n+ samples are mesoporous, and p-type silicon yields meso- to micro-pores. These different morphologies are the result of different pore formation mechanisms. Many mechanisms are thought to contribute to the electrochemical pore growth process in silicon, and the morphology resulting from a given experiment is usually determined by a combination of several of these [23]. Table 1.2 summarizes the types of silicon, the morphologies, and the presumed operative mechanisms for the main types of

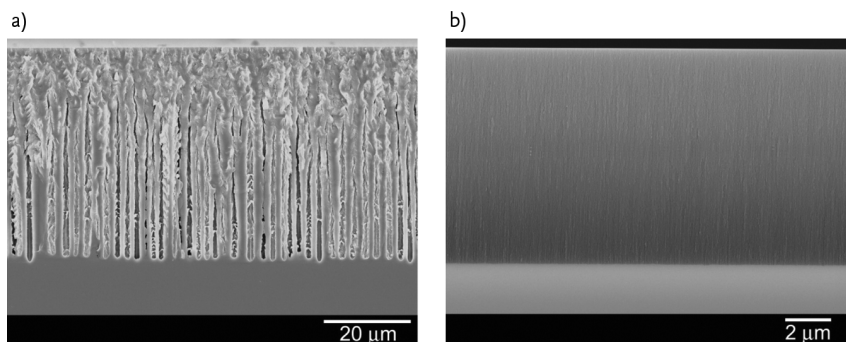


Figure 1.5

Cross-sectional electron micrograph images showing the effect of dopant on pore texture in porous silicon films. Both of these films were prepared under the same conditions of current density (50 mA cm^{-2}), etch time (300 s), and electrolyte composition (3:1 aqueous HF:ethanol). Both samples are etched on the (100) face of the crystal. (a) This is an n-type, luminescent sample, etched by back side illumination. The macropores propagate primarily in the $\langle 100 \rangle$ direction

of the crystal. The porous layer in this image is approximately $50 \mu\text{m}$ thick. (b) This is a highly doped p^{++} -type sample. Note the pores are so small that they are not well resolved in this image, although the general top-to-bottom texturing reflects the $\langle 100 \rangle$ pore propagation direction. This porous layer is $9 \mu\text{m}$ thick. Preparation of these samples is described in the experiments of Chapter 2. Images provided by Luo Gu, UCSD.

Table 1.2 Pore morphologies and formation mechanisms depend on dopant.

| Pore type | Silicon type ^{a)} | Mechanism | Experiment number ^{b)} |
|------------|----------------------------|--|---------------------------------|
| Micropores | p | Crystallographic face selectivity, enhanced electric field, tunneling, quantum confinement | 2.1 |
| Mesopores | p+, p++, n+ | Enhanced electric field, tunneling | 2.2 |
| Macropores | n | Space-charge limited | 2.3 |

a) The superscripts “+” and “++” refer to the level of doping. “+” corresponds to resistivity values of $0.1\text{--}0.01 \Omega \text{ cm}$, “++” corresponds to $0.01\text{--}0.001 \Omega \text{ cm}$ or less.

b) Refers to Experiment number in Chapter 2. Assumes electrochemical etching in HF-containing alcohol/water electrolytes.

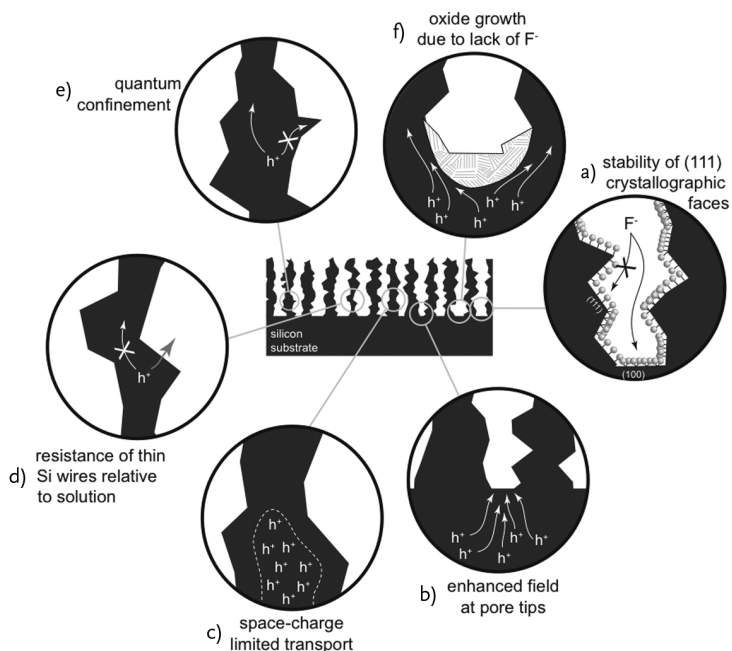


Figure 1.6

Schematic depicting the more important pore-forming mechanisms in porous silicon. (a) The (100) crystallographic face contains strained Si–H bonds, and it tends to be more prone to dissolution compared to other faces. By contrast, the (111) face contains Si–H bonds that are perpendicular to the surface and more stable. The differential reactivity of the crystal faces leads to “crystallographic” pores that propagate primarily in the $\langle 100 \rangle$ direction. (b) The high radius of curvature at the tip (i.e., the bottom) of a pore generates a region of enhanced electric field that attracts valence band holes. (c) The space-charge region is a region in which carriers are depleted due to band bending at the silicon/electrolyte interface. It increases with decreasing dopant density, so this mechanism is a primary determinant of macropore size for low-doped n-type Si. (d) As the diameter of a silicon filament decreases,

its resistance for transport of valence band holes increases. At a critical filament diameter (typically a few nm for p-type silicon), injection of the hole into the solution becomes more favorable, and holes do not propagate further down the length of the nanowire. This mechanism is responsible for the lack of electrochemical dissolution of a microporous layer, once it is formed. (e) The increased band gap resulting from quantum-confinement excludes valence band holes from these smallest regions of the porous silicon matrix. (f) If there are no fluoride ions available at the silicon/solution interface, silicon oxide forms at the interface. Valence band holes are then excluded from this region and they continue to oxidize the silicon/porous silicon interface. This causes pore widening and, ultimately, lift-off of the porous layer (electropolishing).

etches; Figure 1.6 depicts some of the more important mechanisms. In general they can be split into either physical or chemical phenomena.

1.6.1

Chemical Factors Controlling the Electrochemical Etch

The oxidizing equivalents that start the process are valence band holes, driven to the surface by the applied electric field, and by diffusion. The migration of electrons and holes is influenced by the pore morphology; sharp pore tips generate enhanced electric fields that attract charge carriers. Once a valence band hole makes it to a surface Si atom, the atom is susceptible to attack by nucleophiles in the solution, primarily F^- , and H_2O . A simplified reaction mechanism is given in Figure 1.7

The chemistry that occurs at a silicon surface during electrochemical corrosion involves a competition between Si–O, Si–F, and Si–H bond formation. Si–O bonds are chemically attacked by F^- , and significant quantities of Si–O species only form under conditions in which the diffusion of F^- to the silicon surface cannot keep up with the rate of delivery of valence band holes. Such a condition exists, for example, during electropolishing. Electropolishing involves the complete dissolution of silicon without pore formation, and it is observed when the current density is large, or when the HF concentration in the electrolyte is low. When the concentration of HF in the electrolyte is low, oxidized silicon atoms are generated at the surface too rapidly to be attacked by F^- , and water molecules take over the

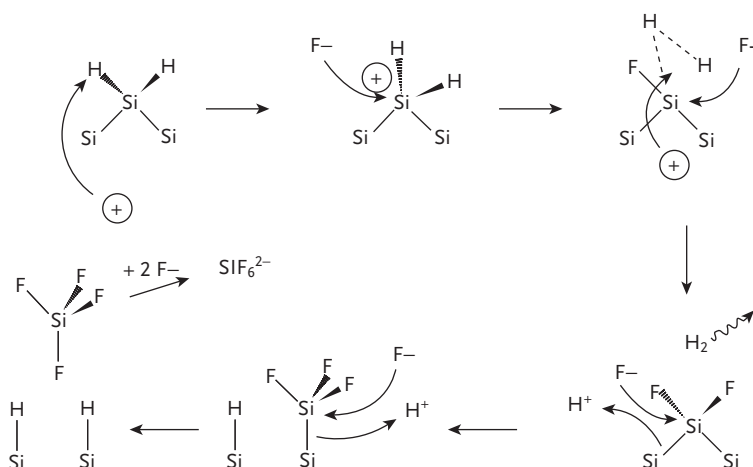
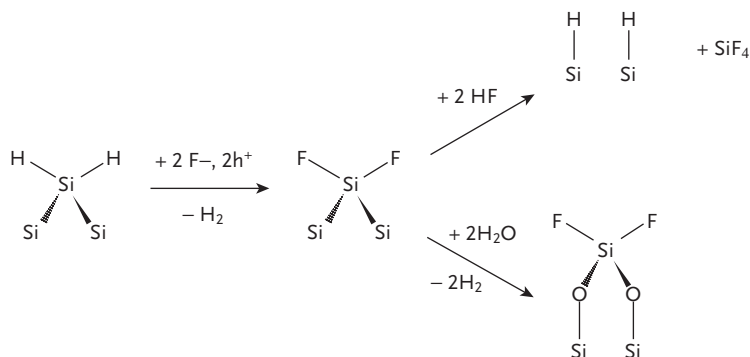


Figure 1.7 Simplified mechanism for electrochemical etching of silicon in fluoride-containing solutions, after [8].

**Figure 1.8**

Electrochemical oxidation of silicon can take two paths, depending on the availability of fluoride ion in the electrolyte. The upper branch depicts oxidation

of silicon when excess HF is present. If the corrosion current exceeds the rate of HF diffusion, water attacks the surface and an insulating oxide is generated [23].

role of nucleophile (Figure 1.8). The reaction mechanism shifts to Si–O formation, and the reaction stoichiometry transitions from 2-electron (Equation 1.9) to 4-electron (Equation 1.6). The lack of fluoride ions means that the oxide cannot be removed from the surface; this insulating oxide terminates propagation of the pore. The valence band holes are then required to move into the porous silicon matrix to oxidize a Si atom that is accessible to the fluoride ions in the electrolyte solution. The result is thinning of the silicon filaments close to the porous silicon/crystalline silicon interface, undercutting the porous silicon layer. An example of the utility of this reaction for generating free-standing, or “lift-off” films of porous silicon is given in Experiment 4.1.

When a silicon wafer is dipped in HF solution, the oxide dissolves and the surface becomes terminated with H atoms. This is puzzling if one considers that Si–F is the most thermodynamically stable bond in all of silicon chemistry; the relative strength of bonds increases in the order Si–H < Si–O < Si–F (Table 1.1). In fact, through the 1980s it was commonly thought that the surface of a silicon wafer cleaned with HF became terminated with Si–F species [24]. It was not until the detailed XPS and FTIR studies of Eli Yablanovitch, Yves Chabal, and others in the 1980s, that the predominance of the hydrides SiH, SiH₂, or SiH₃ was established [25–29]. The reason for the seeming discrepancy is that Si–F bonds are highly polarized due to the large electronegativity of fluorine, and an Si–F surface species is much more susceptible to attack by nucleophiles than an Si–H species. So in a sense, the Si–F bond is too strong; if a fluoride ion attaches to a silicon atom, that atom is rapidly attacked by additional fluoride ions and removed from the surface (Figure 1.7). The surface silicon

atoms capped with H atoms thus predominate on the surface during electrochemical etch: hydrogen is much less electronegative than fluorine, and a surface Si–H species is less susceptible to nucleophilic attack. At the end of an HF etch, porous silicon samples contain primarily Si–H, SiH₂, and SiH₃ surface groups and only traces of O or F.

1.6.2

Crystal Face Selectivity

The most obvious morphological characteristic in most porous silicon samples is the tendency for pores to align along the <100> direction of the crystal (see the next section for definitions of these three-number codes, referred to as Miller indices). This is primarily a chemical effect; so-called “crystallographic pores” are a consequence of the stability of the various crystal faces towards chemical attack. For example the hydrogen-terminated (111) face of silicon is the most stable, with hydrogen atoms bonded directly above a silicon atom (Figure 1.9). Much of the internal nanostructure in porous silicon displays small domains resembling (111) facets.

1.6.3

Physical Factors Controlling the Electrochemical Etch

Physical factors that determine pore morphology primarily involve the electronic properties of the semiconductor: the band structure, the type and concentration of the dopants, the influence growing pores exert in shaping the electric field distribution within the wafer, and quantum confinement effects in the small features identified by the etch. The most important factor at play in pore formation is the availability of valence band holes. This is determined primarily by the dopants, but it is also influenced by illumination, HF concentration, and the magnitude of the applied electric

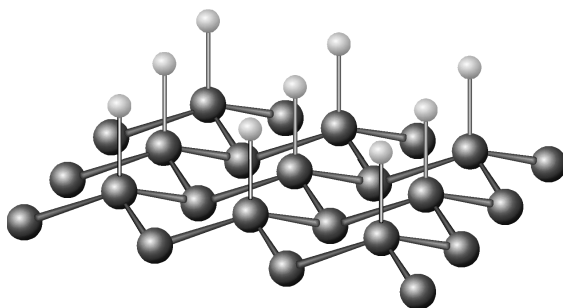


Figure 1.9

The (111) face of a silicon crystal, capped with hydrogen atoms.

field. Whereas crystallographically oriented pores generally form at low current densities and can appear as facet-like structures in cross-sectional scanning electron microscope images, formation of “current-line-oriented-pores”, or “current pores” occurs at higher current densities, and these pores tend to be oriented perpendicular to the surface plane of the wafer. The reason for this is that the equipotential surfaces tend to be parallel to the surface of the wafer, yielding a “path of least resistance” for valence band holes in the perpendicular direction. When the “path of least resistance” for a carrier is sideways through the wall of a pore, pore branching occurs. Current pores (either main or branches) are often nucleated at crystallographic pores [30, 31].

In p-type silicon there is a surplus of valence band holes, and the etch is not limited by their availability. In n-type silicon, however, the scarcity of valence band holes limits the number density of pores in a given area of exposed wafer. During an active etch, there exists a zone near the silicon/electrolyte interface where valence band holes are highly depleted, known as the space-charge region. The pore and wall size is determined by the space-charge region in n-type silicon. The electronic properties of silicon also set the rate and conditions needed for the etch, which are discussed later in this chapter.

1.7 Resume of the Properties of Crystalline Silicon

1.7.1 Orientation

Crystalline silicon possesses a diamond lattice structure, with each silicon atom bonded to four other silicon atoms in a tetrahedral coordination environment. The unit cell is shown in Figure 1.10. Common crystal faces are

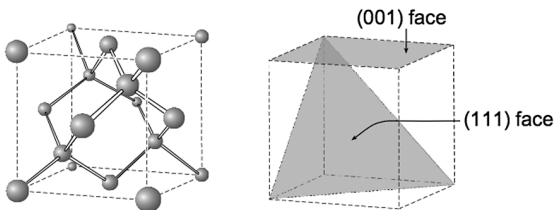


Figure 1.10

The unit cell of silicon. Two of the important crystal faces, with their Miller indices, are shown at the right. The faces of the cube (outlined with the dashed

lines) are all equivalent to (100) faces, due to the cubic symmetry of silicon. The cube diagonals represent (111) faces.

defined by three-number codes, known as Miller indices. The numbers in a Miller index correspond to the inverse of the x , y , and z -axis positions in the unit cell that are intersected by the plane of interest. For example, taking the left rear corner of the cube in Figure 1.10 as the origin of a right-hand coordinate system, the crystal face indicated as the (111) face intersects the cube axes at $x = 1$, $y = 1$, and $z = 1$. The Miller indices for this plane are thus $1/x$, $1/y$, $1/z$, or (111). A plane parallel to an axis intersects it at infinity, so the Miller index would be the reciprocal of infinity, or zero. For example the face labeled with Miller indices (001) in Figure 1.10 intersects the x -axis at infinity, the y -axis at infinity, and the z -axis at 1. Since silicon has cubic symmetry, all six faces of the unit cell are equivalent, and the (100), (010), and (001) faces can all be referred to as (100) faces for convenience. Porous silicon is usually prepared from (100) wafers; that is, wafers polished on the (100) crystal face. Pores display a natural tendency to propagate perpendicular to this face, so when porous silicon is etched from (100) polished wafers, the pores drill vertically into such a wafer.

Crystallographic directions are indicated by defining a vector within the unit cell whose components are resolved with respect to the unit cell axes. The coordinates of the vector are placed in square brackets if a particular direction is being defined, or in angle brackets if a crystallographically equivalent family of directions is being defined. For example, the $\langle 100 \rangle$ direction in the cubic unit cell of Figure 1.10 corresponds to the equivalent directions defined by vectors x , y , z of 100, 010, 001 as well as the negative directions $\bar{1}00$, $0\bar{1}0$, and $00\bar{1}$. These individual directions would be written [100], [010], [001], $[\bar{1}00]$, $[0\bar{1}0]$, and $[00\bar{1}]$, respectively. Thus we would say that the pores propagate primarily in the $\langle 100 \rangle$ direction when a wafer polished on the (100) face is electrochemically etched.

1.7.2

Band Structure

The electronic structure of a molecule can be described as an interaction of atomic orbitals from the individual atoms, which combine to make what chemists call molecular orbitals. Similarly, the electronic structure of a solid derives from atomic orbitals to form what the physicists call energy bands. A key feature of a semiconductor is that the bonding extends over a large distance, often over the entire crystal. The electrons in these orbitals are highly delocalized, making it more convenient to describe bonding in terms of the atomic periodicity in the crystal rather than discrete atomic positions. A complete description is beyond the scope of this book, and we will just give the salient features here. For more detail, there are some good references that describe energy bands from either a chemical [32, 33] or a physical [34] perspective.

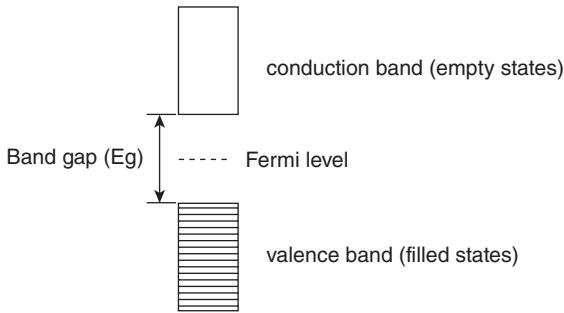


Figure 1.11

Simplified energy band diagram for a semiconductor. The conduction band consists of a series of mostly empty orbitals, while the valence band is made up of orbitals that are mostly filled with electrons. The y-axis in this diagram represents energy, and the band gap represents the energy separating the conduction from the valence band.

Electrons move through the empty orbitals of the conduction band and holes move through the electron vacancies in the valence band. The Fermi level represents the average energy of the mobile charge carriers (both conduction band electrons and valence band holes) in the system.

A simplified energy band diagram for a semiconductor is given in Figure 1.11. The band of states (molecular orbitals) that are occupied by electrons is referred to as the valence band, and the band of empty states is the conduction band. The band gap, or energy gap, is the energy separation between the valence band and the conduction band. The valence band derives its name from the fact that it is occupied by what were the valence electrons of the individual atoms making up the solid. The deeper, or core level electrons are tied to the individual atoms and do not contribute significantly to electrical properties such as conduction. So, for the purposes of charge transport, or conductivity, we are only concerned with these charges that are free to move through the solid, and they are called the mobile charge carriers.

1.7.3

Electrons and Holes

Electrons can be placed in the empty orbitals of the conduction band. Since these electrons are free to move throughout the solid, they contribute to conductivity and thus the origin of the name “conduction band.” If an electron is removed from the valence band, it leaves behind a positively charged empty site. This vacancy is referred to as a “hole.” When a neighboring electron in the valence band moves into this empty site, the space

it vacates becomes a new empty site. This effectively moves the hole in the direction opposite to the travel of the electron. Since the net result is a positive charge moving in the opposing direction, it is convenient to refer to this type of conduction as “hole conduction”. Thus holes exist and travel in the valence band and electrons travel in the conduction band. Both of these mobile charge carriers can contribute to conductivity in a semiconductor. The Fermi energy is defined as the average energy of all of the mobile charge carriers in the system (both electrons and holes), and its value is represented by the Fermi level, shown with a dashed line in Figure 1.11.

Conductivity is related to the concentration of mobile charge carriers in a semiconductor, and there are four basic ways to increase these concentrations: First, you can heat the sample. This will thermally promote electrons from the valence band to the conduction band, generating an equal number of valence band holes and conduction band electrons. At any temperature greater than absolute zero, there are a finite number of electrons with sufficient energy to jump the band gap. There is always a small contribution to conductivity from this thermal process, and it is the reason that sensitive semiconductor-based light detectors, such as photodiodes and CCDs (charge coupled devices) need to be cooled to reduce noise in their signals. Second, you can shine light on the sample. Light with energy greater than the bandgap energy will promote an electron from the valence band to the conduction band, simultaneously generating a conduction band electron and a valence band hole. Third, you can dope the sample with an impurity that donates one of its electrons to the conduction band of the semiconductor or accepts an electron from the valence band. Fourth, you can inject electrons or holes from a material placed in contact with the semiconductor. For example, a transistor operates by injection of carriers from a “gate” electrode into a region of semiconductor that is devoid of carriers. The next sections discuss the two mechanisms for increasing carrier concentration that are most relevant to this book: photoexcitation and doping.

1.7.4

Photoexcitation of Semiconductors

The energy to promote an electron from the valence to the conduction band can also be supplied by a photon of light, provided its energy exceeds the band gap energy. There are well-defined selection rules for this process, and one of the key requirements in crystalline silicon is that the photoexcitation event be accompanied by a lattice vibrational quantum, that is, a phonon. Semiconductors that require phonon absorption for photoexcitation are *indirect gap* semiconductors, and those that do not are *direct gap* semiconductors. Silicon is an indirect gap semiconductor. This phonon constraint has important ramifications in processes that involve absorption

of light, such as photoetching of n-type silicon or direct photopatterning of porous silicon during fabrication. Because an indirect gap transition is a two-body problem (photon and phonon transitions must take place simultaneously), it has a low probability. This translates into a small extinction coefficient. For example, on average a red photon will penetrate about $7\ \mu\text{m}$ into silicon before it is absorbed, whereas, in gallium arsenide, a direct gap semiconductor, the penetration depth is less than 700 nm.

1.7.5

Dopants

Dopants, sometimes called impurities, are elements added to a semiconductor to increase its conductivity. The element chosen to act as a dopant generally has one extra or one less valence electron than the semiconductor. For example, phosphorus lies to the right of silicon in the periodic table, and so it has one more valence electron than silicon. It is added to the molten Si during production, and it replaces a Si atom in the crystal lattice. In the language of solid state chemistry, this is referred to as a substitutional defect. The extra electron is donated to the conduction band, increasing the conductivity of the semiconductor. Similarly, a boron atom substituted into the lattice increases conductivity by donating a hole to the valence band.

Electrons and holes are referred to as charge carriers, because they carry charge (current) through the semiconductor. Keep in mind the term “holes” here is the electronic term, referring to an electron vacancy in the valence band rather than a physical void. Dopants generate an excess of one type of charge carrier; the “n” in “n-type” refers to a negatively charged carrier, that is, an electron, while the “p” in “p-type” refers to the positively charged hole. Undoped silicon has an equal number of electrons and holes due to intrinsic ionization of the pure material, and it is called “intrinsic” silicon. Dopants for Si are generally either phosphorus (for n-type doping) or boron (for p-type doping). Due to the solubility limits of phosphorus, highly doped n-type wafers sometimes use antimony (Sb) as a dopant. Do not confuse the element symbol for phosphorus (P) with the indication of dopant type; phosphorus-doped silicon is n-type. Manufacturers will usually spell out the element name to avoid confusion. For example, a packing label on a wafer box will say “type: P, dopant: boron” to indicate a p-type lot, or “type: N, dopant: phosphorus” to indicate n-type wafers. You should check for both descriptors to be sure you are using the intended material.

Under normal conditions, electrons and holes are in equilibrium with each other in a semiconductor, and you cannot increase the concentration of one of these carrier types without decreasing the concentration of the other. If you increase the concentration of electrons (by adding a

phosphorus dopant, for instance), some of the excess electrons will recombine with the available holes to establish a new equilibrium. There is a form of the law of mass action, equivalent to the equilibrium relationship between H^+ and OH^- in aqueous solutions, described by Equation 1.10:

$$n \cdot p = n_i^2 \quad (1.10)$$

where n and p are the concentrations of mobile electrons and holes, respectively, and n_i is a constant, representing the equilibrium constant for electrons and holes in the semiconductor. It is temperature dependent; for silicon at room temperature, $n_i = 1.45 \times 10^{10} \text{ cm}^{-3}$. This value represents the equilibrium concentration of electrons or holes in a pure (undoped, or intrinsic) silicon crystal.

1.7.6

Conductivity

Conductivity measures the ability of a material to carry electrical current, which is the transport of charge. Resistivity is the inverse of conductivity, measuring the propensity of the material to impede charge transport. For any material conductivity generally relies on two parameters: the concentration of the charge carriers (electrons and holes), and the mobility of these carriers. Whereas any material has plenty of electrons in the valence and core levels of its atomic constituents, if the electrons are not free to move from one spot to the next the material cannot conduct electricity. The basic relationship between conductivity (σ), carrier mobility (μ_n, μ_p), and carrier concentrations (n, p) is given by Equation 1.11

$$\sigma = q(\mu_n n + \mu_p p) \quad (1.11)$$

Representative room-temperature mobility values for silicon are $\mu_n = 1300 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and $\mu_p = 450 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. An example of the use of Equations 1.10 and 1.11 to calculate carrier concentrations in a sample of known resistivity is given in Experiment 1.1.

1.7.7

Evolution of Energy Bands upon Immersion in an Electrolyte

When a metal contact is made to a silicon wafer, a small number of electrons will pass between the two materials to equilibrate the work functions. If the work functions of the two materials are of the appropriate values, a build-up of fixed charge at the interface results. This interfacial charge acts as a barrier for transport of additional electrons. Differences in dielectric constant and density of states between the two materials lead to an asymmetric barrier, resulting in the unidirectional, or rectifying electron trans-

port behavior commonly observed with a diode. For a metal/semiconductor contact, the built-in field is referred to as a Schottky barrier.

A similar situation to Schottky barrier formation occurs when a silicon electrode is immersed in an electrolyte. Charge equilibration between the two phases leads to a barrier that either blocks or allows current to flow, depending on the direction of the current. The energy band diagrams of Figure 1.12 show the situation before and after immersion of n-type and p-type silicon electrodes into electrolyte. The barrier is depicted as a bending of the conduction and valence bands in the vicinity of the interface. In the energy band diagrams, it is energetically favorable for holes to move upwards along the band lines because of their positive charge, and electrons

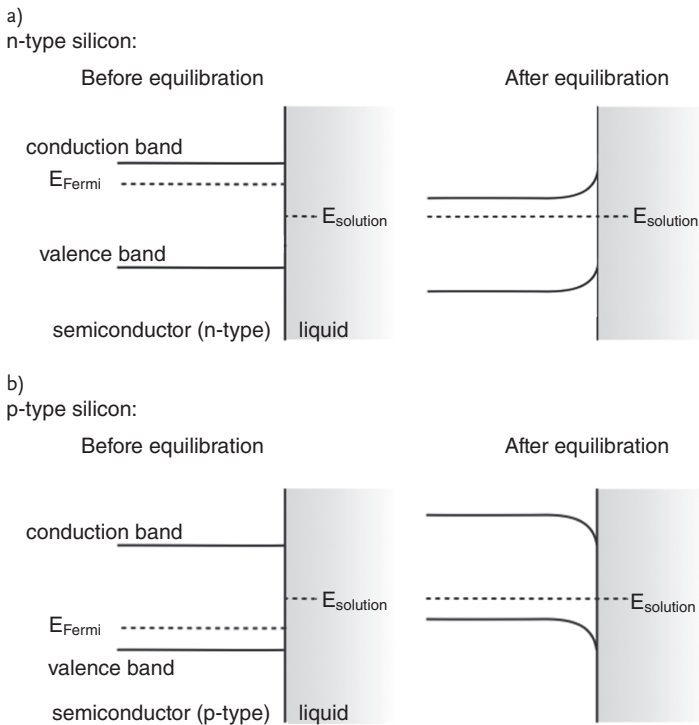


Figure 1.12

(a) Equilibration of charge at the semiconductor/electrolyte interface for an n-type semiconductor. The evolution of the energy band structure that occurs upon immersion in a liquid is depicted. The y-axis in this diagram is energy, and the spatial dimension through the semiconductor/electrolyte interface is depicted along x. The energy bands bend

in the vicinity of the interface as a result of charge equilibration between the semiconductor and the liquid phase.

(b) Equilibration of charge at the semiconductor/electrolyte interface for a p-type semiconductor. The energy bands bend as a result of charge equilibration between the semiconductor and the liquid phase.

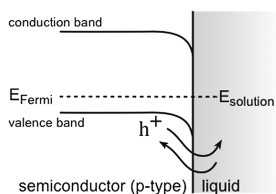


Figure 1.13 Charge transport processes at the semiconductor/electrolyte interface for a p-type semiconductor. The increase in hole current across the interface under forward bias (silicon positive relative to

the Pt counter-electrode in solution) is depicted. The bent energy bands provide an impediment to charge transfer that is overcome with a small applied bias.

will spontaneously move downwards. A common mnemonic is to think of holes as bubbles that float upwards and electrons as balls that roll downwards along the energy band lines in these diagrams.

1.7.8

Charge Transport at p-Type Si Liquid Junctions

Valence band holes are the important charge carriers that lead to electrode corrosion. For a p-type silicon sample, these are the majority carriers. With no applied bias, the rate of hole transport in either direction across the interface is small, as depicted in Figure 1.13. When a positive bias is applied to the silicon electrode, the barrier to interfacial charge transport is reduced and valence band holes begin to accumulate at the interface. In the language of solid state electronics, we would say that the diode is in forward bias. The holes participate in the corrosion reactions of Equation 1.6 or 1.9, and porous silicon begins to form.

If the potential of the silicon electrode is adjusted to be negative of the solution potential, the diode goes into reverse bias. The situation depicted in Figure 1.14 occurs. The barrier to hole transport to the interface increases, and the corrosion reaction is effectively shut off.

1.7.9

Idealized Current–Voltage Curve at p-Type Liquid Junctions

The idealized current–voltage curve for a p-type silicon wafer in an HF electrolyte is shown in Figure 1.15. The p-silicon/electrolyte junction is in forward bias during etch, so the current will increase exponentially with even a small increase in applied voltage. The mathematical relationship for the current–voltage curve of an ideal diode is also given in the figure. Note

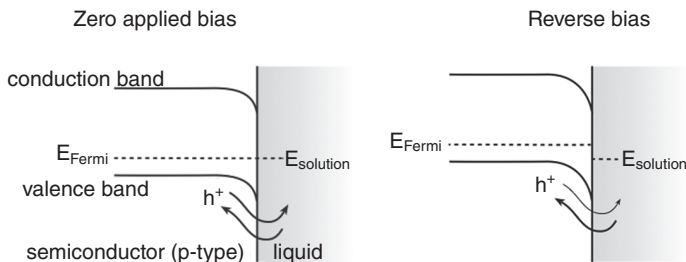


Figure 1.14
Blocking of charge transport across the semiconductor/electrolyte interface under reverse bias conditions for a p-type semiconductor. A decrease in the interfacial transport of holes occurs when

the semiconductor is placed under reverse bias conditions. In this situation, only a small leakage current (reverse saturation current) flows into solution.

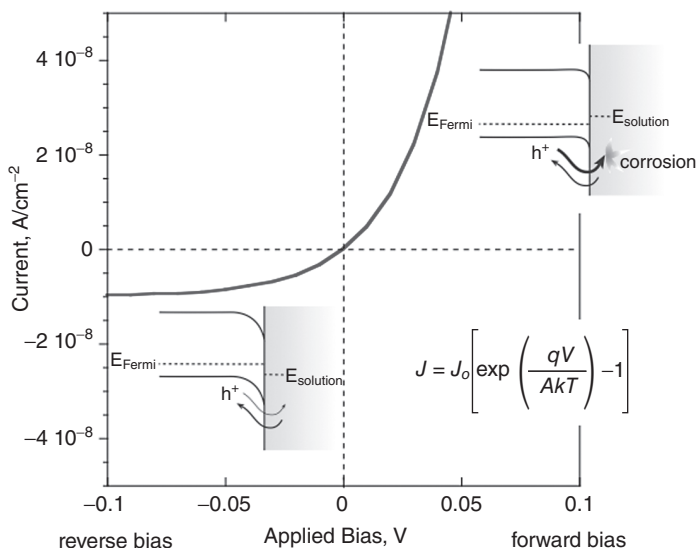


Figure 1.15
Ideal Diode Law applied to electrocorrosion of a p-type liquid junction. Under forward bias (right-hand side of the plot), the corrosion (hole) current turns on exponentially. Under reverse bias conditions, the hole current across the

semiconductor/electrolyte interface is limited to the value of the reverse saturation current density, J_0 . Etching proceeds when the system is in forward bias.

the similarity of this curve to the first part of the curve in Figure 1.3 (in the porous silicon formation region). The ideal curve of Figure 1.15 is only approximately correct for electrochemical corrosion of silicon. As porous silicon forms, the defect density at the interface increases, degrading the quality of the junction.

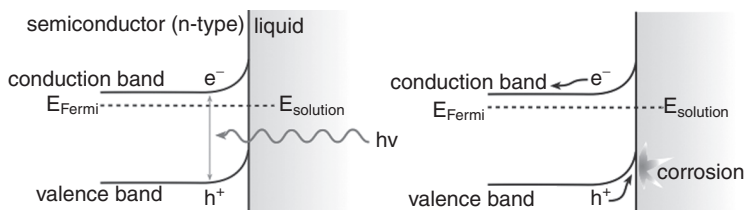


Figure 1.16

n-type Si must be illuminated in order to drive electrocorrosion. Light generates electron-hole pairs. For n-type Si, the built-in field sweeps the valence band

holes to the semiconductor/electrolyte interface, where they supply the oxidizing equivalents for the corrosion reaction.

1.7.10

Energetics at n-Type Si Liquid Junctions

Holes are the important charge carriers that lead to electrode corrosion. Because the band bending at an n-type semiconductor electrode is opposite to that of a p-type electrode (Figure 1.12), hole current at the n-type interface is blocked by the junction. The majority of carriers in an n-type semiconductor are electrons; to generate a sufficient number of holes to carry out the corrosion reaction, the semiconductor must be illuminated. Light generates electron-hole pairs near the semiconductor interface, and the built-in field sweeps the holes to the surface. This is depicted schematically in Figure 1.16.

1.7.11

Idealized Current-Voltage Curve at n-type Liquid Junctions

The idealized j - V curve for an n-type semiconductor in contact with an electrolyte is shown in Figure 1.17. Two traces are shown, one for an electrode in the dark and the other for one under illumination.

1.8

Choosing, Characterizing, and Preparing a Silicon Wafer

When purchasing crystalline silicon wafers (Figure 1.18), you must specify three main properties: the cut (crystal orientation) of the wafer, dopant type, and resistivity. All three of these parameters are crucial in determining the size, number, and direction of the pores that will be generated in your porous silicon samples. In addition, there are several other properties that

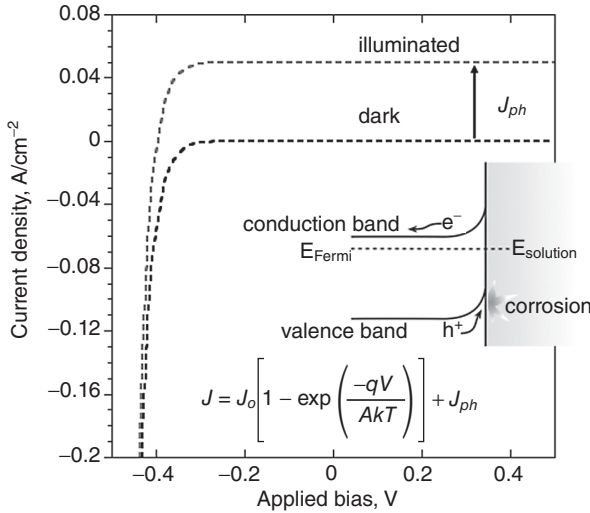


Figure 1.17

Current–voltage curves for an n-type liquid junction. For an n-type junction, the corrosion (hole) current is blocked by the diode. Corrosion is induced by illumination of the semiconductor, which generates an excess of holes. The built-in field of the diode draws the holes to the interface, where they contribute to corrosion of the electrode surface. The

equation for the Ideal Diode Law, incorporating the effect of photocurrent (J_{ph}), is shown. Under reverse bias conditions, the hole current across the semiconductor/electrolyte interface is limited to the sum of the reverse saturation current and the photocurrent, $J_0 + J_{ph}$.

you should understand when working with silicon. Those parameters usually given by the wafer vendors are presented in Table 1.3. We described the key structural and electronic properties underlying the parameters relevant to the preparation of the various porous silicon morphologies in the previous sections. In the following we describe the techniques used to characterize the crystalline silicon starting material. There are many good references that provide more detailed discussion. One of the most useful is [35].

1.8.1

Measurement of Wafer Resistivity

One of the biggest problems in the measurement of resistivity of a material is contact resistance between the probe leads and the sample. For example, a silicon wafer usually has about 7 nm of native oxide on its surface. If you place the two leads of an ohmmeter (multimeter set to “Ohms” setting) on the surface of a silicon wafer, the resistance value you measure is

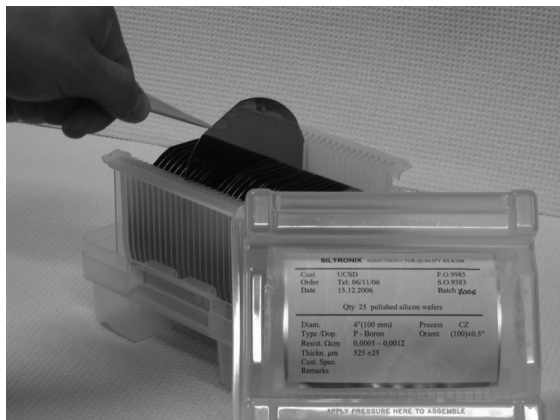


Figure 1.18

Crystalline silicon wafers, fresh out of the box from the vendor. The three most important properties are crystal orientation, dopant type, and resistivity. Wafers are generally shipped in polypropylene containers and should be handled with nylon or other plastic tweezers. Impurities from fingerprints or metallic tweezers can influence the outcome of various

processing steps such as etching or thermal treatment. These wafers are 6 in diameter, p-type wafers, polished on the (100) surface, doped to a very high concentration with boron. With a nominal resistivity of $0.001 \Omega \text{ cm}$, these wafers would be considered degenerately doped, designated p^{++} type Si.

dominated by this highly resistive SiO_2 layer, even if the underlying silicon is highly conductive. The four-point probe method eliminates the effect of contact resistance. The four-point experiment is pictured schematically in Figure 1.19 and photographically in Figure 1.20.

A constant current is passed between the outer two probe tips, while the voltage drop is simultaneously measured between the inner two tips using a high impedance voltmeter. Resistivity is determined from the measured values of voltage drop (V) and current (I)

The sheet resistance (R_s) is calculated from the ratio of current to voltage, multiplied by a correction factor that is related to the sample geometry:

$$R_s = \frac{V}{I} \cdot CF \quad (1.12)$$

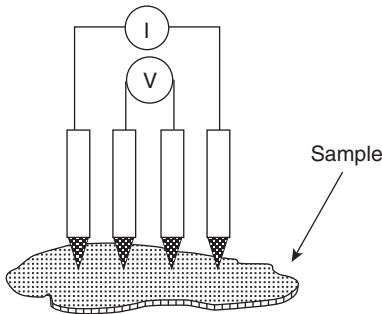
Where V is in volts and I is in amps. The value of CF is 4.54 for an infinite sheet (this approximation is valid if the sample is over a factor of 10 larger in both the x - and y - directions than the probe tip spacing). The units of sheet resistance are ohms per square.

Sheet resistance and resistivity (ρ) are related by:

$$\rho = R_s W \quad (1.13)$$

Table 1.3 Typical crystalline silicon wafer parameters specified by the manufacturer.

| Parameter | Description | Example |
|-------------|---|---|
| Orientation | Miller index of the wafer, indicates which crystal face is located on the face of the wafer | $\langle 100 \rangle$, polished on the (100) face. Most commonly used for porous Si preparation. Note the direction of pore propagation is primarily in the $\langle 100 \rangle$ direction; etching a (100) wafer will yield pores perpendicular to the surface. If you choose a (110) wafer by mistake, you will get a cross-hatching of pores, propagating at angles of 45° from the surface normal. |
| Type/dopant | Type of doping (n or p) and chemical element used to dope the wafer | P-Boron. Boron is the dopant; it generates a p-type impurity |
| Resistivity | The electrical resistivity of the wafer, related to the dopant concentration | 0.0005–0.0012 Ω cm. Manufacturing is never perfect; a range of values is usually specified. You should always verify with a 4-point probe measurement. |
| Thickness | Thickness of the wafer | $525 \pm 25 \mu\text{m}$. |
| Process | Method used to grow the silicon crystal | CZ. Grown using the standard Chockraszki method. Very high quality (and expensive) wafers are grown by the float zone method, designated FZ. |

**Figure 1.19** Schematic diagram of the four-point resistivity experiment.

Where W is the thickness of the wafer being measured. The usual units of resistivity are ohm cm (Ω cm) so the thickness should be measured in cm. You should not trust the nominal wafer thickness quoted by the manufacturer on the box because thickness can differ significantly from wafer to wafer in a given lot.

EXPERIMENT 1.1: Measure the resistivity of a silicon wafer

In this exercise, you will measure the resistivity of a silicon wafer using a four-point resistivity probe. You will then calculate the dopant concentration in the wafer using the ideal mobility relationship.

Equipment needed:

| | |
|---|---|
| 4-point resistivity probe | Complete probe stations are available from many manufacturers. A simple test station like the Alessi CPS resistivity test fixture with a C4S 4-point probe head (available from Cascade Microtech, www.cascademicrotech.com) is a good option. |
| Constant current source, voltmeter, ammeter | All-in-one packages, such as the Keithley 2001 multimeter, (www.keithley.com) that source a current, measure the voltage drop, and output a resistance value (“4-wire resistance measurement”) are a simple solution. Alternatively, a power supply that can supply a constant current (B + K Precision 1623A, www.bkprecision.com) and two digital multimeters (Fluke 187, www.fluke.com), one configured to measure current, the other to measure voltage, can be used. |
| Digital micrometer | Mitutoyo 293-832, (www.mitutoyo.com) |

Procedure:

- 1) Measure the resistivity of the sample using the 4-point probe. Make 5 measurements in 5 separate spots on the wafer, and report the average value. Be sure that all of the test spots are at least 10 times as far from the edge of the wafer as the spacing of the probe tips. An example of the connections appropriate for the Keithley model 2001 DMM is shown in Figure 1.20
- 2) Depending on your specific measurement apparatus, you will have either pairs of voltage and current readings or you will have individual “4-wire resistance” values, where the ratio of V/i has already been calculated for you. Examples of both are shown in the table below.
- 3) Measure thickness of sample with the micrometer. Note this will scratch the surface of your sample, which can affect the quality of the porous Si formed in the vicinity.

To calculate resistivity:

- a) Convert resistance measurement (V/i) to sheet resistance, R_s :

$$R_s = \frac{V}{i} \cdot CF$$

- b) where $CF = 4.532$ (infinite sheet approximation)
 c) Convert R_s to resistivity:

$$\rho = R_s \cdot W$$

- d) where W = your wafer thickness, in cm (measure with micrometer)

Results:

Values are given below for a representative sample.

Sample thickness = 0.0537 cm

| | Voltage, V (mV) | Current, i (mA) | V/i (Ω) | R_s (Ω per square) | Resistivity (Ω cm) |
|-----|--------------------|----------------------|--------------------|---------------------------------|-------------------------------|
| 1 | 0.038 | 8.530 | 0.00445 | 0.02019 | 0.00108 |
| 2 | 0.038 | 8.529 | 0.00446 | 0.02019 | 0.00108 |
| 3 | 0.038 | 8.525 | 0.00446 | 0.02020 | 0.00108 |
| 4 | 0.038 | 8.532 | 0.00445 | 0.02019 | 0.00108 |
| 5 | 0.037 | 8.545 | 0.00433 | 0.01963 | 0.00105 |
| Avg | 0.0378 | 8.532 | 0.00443 | 0.02008 | 0.0011 |

Sample resistivity = 1.1 m Ω cm

The simplified relationships for conductivity and carrier concentration are given in Equations 1.10 and 1.11. Using the mobility values $\mu_n = 1300 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and $\mu_p = 450 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, the intrinsic silicon constant $n_i = 1.45 \times 10^{10} \text{ cm}^{-3}$, and $q = 1.602 \times 10^{-19} \text{ C}$, the concentrations of electrons and holes in this sample can be calculated:

$$\sigma = \frac{1}{\rho} = q(\mu_p p + \mu_n n)$$

assuming $n \ll p$,

$$p = \frac{1}{\rho q \mu_p} = 1.3 \times 10^{19} \text{ cm}^{-3}$$

$$n = \frac{n_i^2}{p} = 17$$

Note, in this very highly doped semiconductor the concentration of free electrons is negligible (~ 17) and all the current is carried by valence band

holes. This calculation assumed $p \gg n$; as you can see, a fair assumption for this particular sample. If the carrier concentrations are closer to each other (low-doped n- or p-type material), you have to solve the problem using the binomial expansion.

If we assume that all the boron dopant atoms in the semiconductor can be ionized to donate a hole to the valence band, the dopant density (in atoms cm^{-3}) is equal to the value of p , or $1.3 \times 10^{19} \text{ cm}^{-3}$. This corresponds to a boron concentration of 200 ppm (200 B atoms per 10^6 Si atoms) in the Si crystal. So, even with very highly doped silicon, the dopant atoms represent a very small fraction of the overall composition.

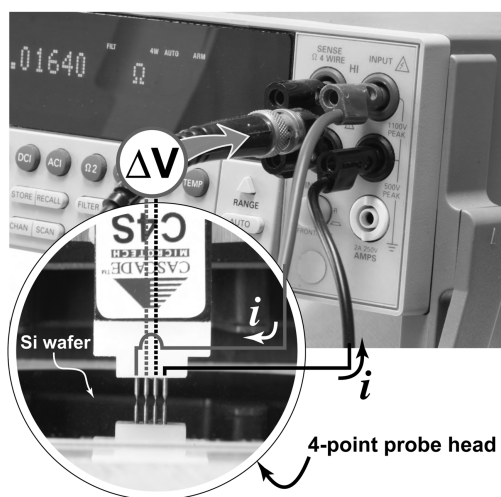


Figure 1.20

Connections for a 4-point probe measurement of wafer resistivity using the Keithley 2001 DMM (www.keithley.com) in the four-wire resistance mode. Inset shows a 4-point probe head in contact with a polished silicon wafer, and the electrical connections are depicted. Specific procedure to measure resistivity of a wafer using this unit: (a) Power on, (b) press “Ω4” button, (c) press “config”

button, (d) Speed: “HiAccuracy”, (e) filter: 25 (this is the number of measurements to average), (f) resIn: “7.5 d”, (g) OffsetComp: “on”, (h) Exit, (i) put copper foil on the stage, place probe tips in contact, (j) press “rel” to zero reading, (k) replace the copper foil with your sample. Measure your sample in 5 spots. Toggle “filter” button to turn on and off averaging between measurements.

1.8.2

Cleaving a Silicon Wafer

During manufacture, silicon wafers are cut from a large single crystal (known as a boule) with a diamond saw. The angle of the cut is chosen to coincide with a particular crystal face, and this face is then polished to a

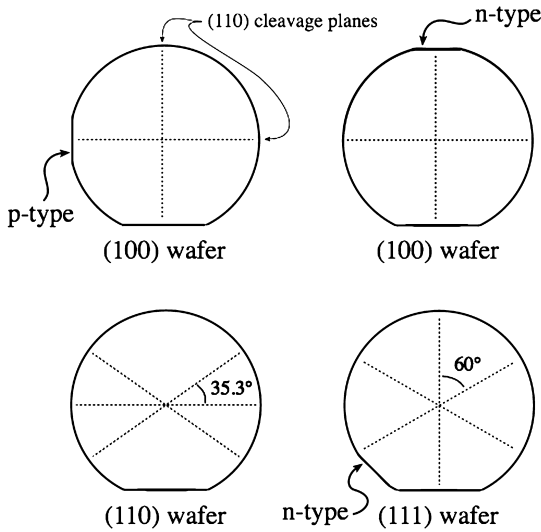


Figure 1.21

Silicon wafers and the meaning of the fiducial flats, as adopted by the SEMI Standards organization (www.semi.org). Dashed lines indicate the location of the (110) natural cleavage planes in the wafer. For n-type, (100) wafers, there are 2 flats: the major flat is parallel to the (110) cleavage plane, the second flat is parallel to the major flat, on the opposite side of the wafer. For p-type, (100), there are 2

flats: the major flat is parallel to the (110) cleavage plane, the second flat is at 90° from the major flat. For n-type, (111), there are 2 flats: the major flat is parallel to (110), the second flat is 45° from the major flat. For p-type, (111), there is only 1 major flat. For wafers with diameters >200 mm, the orientation is indicated with a notch instead of a flat. Adapted from [35].

mirror finish. The wafer is a round disc, though the orientation of other crystal planes relative to the polished face is indicated by flats cut into the wafer, as indicated in Figure 1.21. These markings allow one to find the (110) natural cleavage planes of silicon.

Silicon will break easily along these natural cleavage planes of the crystal. To break a wafer into squares of the appropriate size for the experiments in this book, it helps to scribe a small notch or groove on the back (unpolished) side of the wafer first. A diamond or tungsten carbide scribe can be used (Fisher Scientific, www.fishersci.com, cat # 08-675). The following technique can be used:

- 1) Place the wafer polished side down on a clean, dust-free tissue paper to protect the surface
- 2) Place a straight edge on the back side of the wafer, parallel to one of the cleavage planes. The line should be placed to produce a strip of silicon approx 2 cm wide

- 3) Using the scribe and the straight edge as a guide, score a line. Go over the line several times with the scribe to ensure the groove is deep enough to yield a good cleave
- 4) Flip the wafer over onto a stack of 10–20 paper towels, place a clean tissue onto the polished face
- 5) Place a round stick, such as a pencil, on the wafer parallel to and directly over the scored line.
- 6) Apply gentle, even pressure to the stick until the wafer cracks. It should crack along the length of the score.
- 7) Repeat the procedure to make 2 cm squares. The squares should be a few mm larger than the O-ring used in the etching cell, to ensure a leak-free seal.

Wafers can also be cleaved without placing a score on the back side, although it takes a little more practice. Place the wafer on top of a single tissue on a hard, flat surface. Using a razor blade, apply firm pressure to the edge of the wafer and pull the blade off the edge until it snaps to the surface of the table. A crack should propagate along the (110) cleavage plane. With a little practice, this is much faster than the scoring method.

1.8.3

Determination of Carrier Type by the Hot-Probe Method

Although the manufacturer will specify the carrier type (n or p), it is sometimes necessary to verify this. The hot-probe measurement is a simple method to distinguish between n- and p-type semiconductors (Figure 1.22).

1.8.4

Ohmic Contacts

In order to etch a silicon wafer, a low-resistance contact must be made to the back side of the wafer. For highly doped substrates ($<0.1 \Omega \text{ cm}$), a metal foil (aluminum or platinum) placed in contact with the wafer is sufficient. When etching p- or n-type silicon with resistivity ($>0.1 \Omega \text{ cm}$), the metal forms a rectifying junction, generating a barrier to electron transport that leads to irreproducible and non-uniform porous layers. The rectifying junction acts like a Schottky diode, illustrated in Figure 1.23, with the relevant equivalent circuits shown.

In addition to the rectifying nature of some metal contacts, a metal (e.g., alligator clip or aluminum foil) pressed against silicon will generally have some contact resistance associated with the oxides coating the surfaces of

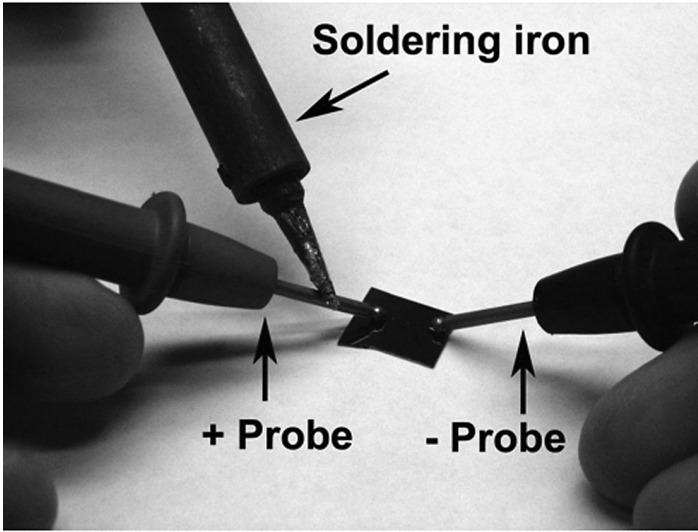


Figure 1.22

Hot probe measurement of carrier type. The sign of the voltage difference between a probe heated with a soldering iron and one at ambient temperature identifies whether a chip is n- or p-type. When the black lead shown on the right is

connected to the ground input on the DMM, a positive voltage indicates an n-type wafer; negative voltage indicates p-type. It helps if you have three hands available for this measurement.

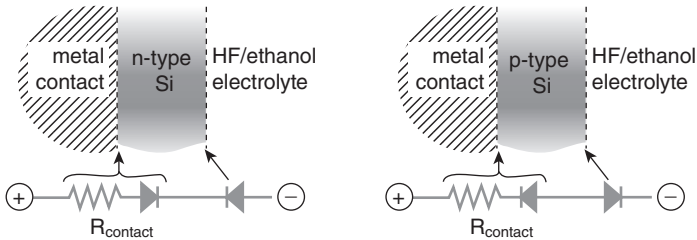


Figure 1.23

The contacting interfaces and the corresponding equivalent circuits for etching of n- and p-type Si. In either case, the diodes corresponding to the metal–Si and the Si–electrolyte junctions are opposing. In order to pass significant current through the p-type

semiconductor, the metal–silicon contact must be close to ohmic. In order to pass significant current through the n-type semiconductor, the silicon–electrolyte junction must be illuminated in order to generate photocurrent.

EXPERIMENT 1.2: Hot probe determination of the carrier type in a silicon wafer

In this exercise, you will determine the carrier type in a silicon wafer using a soldering iron and a multimeter.

Equipment needed:

| | |
|--------------------------|---|
| Digital multimeter (DMM) | For this experiment you will need a meter with a floating ground, to avoid establishing a ground loop with the soldering iron. Use of a battery-powered DMM will do the trick. The Fluke 187 (www.fluke.com) is a good choice. |
| Soldering iron | Weller SPG40 |

Procedure:

Choose either an n- or a p-type piece of Si. Set the DMM to the lowest DC voltage setting (mV on the Fluke 187). Place the two probes on the chip and touch the hot soldering iron to the probe leading to the + input (red V) of the DMM. After a few seconds, note the sign of the voltage reading.

Results:

For sample resistivities in the $1 \Omega \text{ cm}$ range, you should observe a voltage difference of 50–100 mV, depending on how hot the probe gets. For an n-type sample, the sign of the voltage will be positive; for a p-type sample, the sign will be negative. You should move the iron from the + to the – lead of the DMM and observe a change in the sign of the voltage to test the consistency of the measurement—dirty probe tips can give a false reading.

both the metal and the silicon electrode. The practical consequence of either junction formation or contact resistance is that the etching power supply must work harder to push the desired current through the silicon/electrolyte interface. This means it must supply more voltage. The power supplies listed in Table 2.1 can all supply the voltage sufficient for most experiments, though there may be undesired consequences if the contact resistance gets too high. As mentioned above, irreproducible or nonuniform pore morphologies are the most common result. For some of the experiments performed in this book we ignore the effects of the junction and just let the power supply do the work. However, in many cases it is appropriate to make an ohmic contact to the wafer before etching, in particular for p-type silicon.

An ohmic contact is defined as a metal–semiconductor junction that has negligible contact resistance relative to the resistance of the bulk semiconductor. To make such a contact, the interfacial resistance and/or rectifying nature of the silicon/metal interface must be destroyed. It is generally accomplished by evaporating a metal with a Fermi energy appropriate to produce a low Schottky barrier. Alternatively, physical abrasion generates surface defects that act as efficient carrier recombination centers, negating the rectifying properties of the junction.

In order to make a good back-contact to the silicon wafer in an etching cell, you should:

- 1) Remove the native oxide from the back of the wafer by soaking or rinsing the back side of the wafer in 3:1 48% aqueous HF:ethanol solution for 10–30s before mounting it in the cell. Rinse with ethanol and dry.
- 2) Make sure to use a clean (platinum or aluminum foil) back-contact.
- 3) Make sure the clips used to connect the back-contact and the platinum counter-electrode are clean and in good shape. After time, exposure of copper or brass alligator clips to the corrosive HF fumes will destroy them.

It is a good idea to monitor the voltage being applied by the power supply during etch. It should be between 0.5 and 5V, typically. If the applied voltage is >5V—or worse: pushing close to the maximum voltage the source can supply—you will probably get irreproducible results (lower porosity than expected, thinner film, unusual layered structures, different optical properties, etc.) If you see strange results, you can troubleshoot the etching rig by systematically testing all the contacts using a digital multimeter. If it is clear that the problem is the metal–silicon contact, you need to make an ohmic contact to the wafer.

1.8.4.1 Making an Ohmic Contact by Metal Evaporation

For an ohmic contact to n-type silicon, a gold–antimony (Au–Sb) alloy containing 0.1% Sb is evaporated onto the wafer (remove the native oxide from the wafer with HF solution first, see above), and then the wafer is annealed at 300°C in an inert (vacuum, N₂ or Ar) atmosphere for 3h.

For an ohmic contact to p-type silicon, a thin layer of aluminum is placed on the wafer by either sputter-coating or by e-beam evaporation. A standard recipe for sputter-coating is:

- 1) Clean the side to be contacted using an RCA etch.
- 2) Sputter-coat the wafer using a commercial sputter-coater (Rotation: 65, pressure: 2.6–2.7 mtorr, Ar gas flow: 35 SCCM, power: 150 W, time: 15 min (yields approx. 200 nm thick film).

A standard recipe for electron beam evaporation:

- 1) Clean the side to be contacted using an RCA etch.
- 2) Deposit at a rate of 0.2 nm s^{-1} to 200 nm thickness.

For either e-beam evaporation or sputter coating, samples must be thermally annealed in an inert atmosphere or in vacuum (150°C for 2 min, then 450°C for 15 min).

1.8.4.2 Making an Ohmic Contact by Mechanical Abrasion

A quick, brute force method of making an ohmic contact to either n- or p-type Si is to place a small amount of 1:1 gallium/indium (Ga/In) eutectic on the back side of the wafer and work it into the surface by scratching with a razor blade or carbide scribe until the entire back surface is shiny. The low work function of the eutectic makes it a good ohmic contact to n-type Si, although scratching generates so many interfacial defects that it works pretty well for p-type too. Gallium and indium are toxic, so the samples must be handled with care. After application, the eutectic can be coated with silver paint (SPI Supplies, # 05001-AB, www.2spi.com) to protect it.

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