Chapter 2

Digital Phase Lock Loops

2.1 Introduction

The analog PLLs (APLLs) are still widely used, but digital PLLs (DPLLs) are attracting more attention for the significant advantages of digital systems over their analog counterparts. These advantages include superiority in performance, speed, reliability, and reduction in size and cost. DPLLs alleviated many problems associated with APLLs. The following is a brief comparison:

1. APLLs suffer from the sensitivity of the voltage-controlled oscillator (which decides the center frequency) to temperature and power supply variations, hence the need for initial calibration and periodic adjustments. DPLLs do not suffer from such a problem [12, 17, 68].

2. The most familiar error detectors used in APLLs utilize analog multipliers (balanced modulators) which are sensitive to d.c. drifts [10, 18], a problem that does not exist in DPLLs.

3. DPLLs can operate at very low frequencies that create problems in APLLs [17, 18]. These problems are related to the operation of the analog low-pass filter in extracting the lower frequency component [11, 18],as it needs larger time for better frequency resolution, and this will reduce the locking speed.

4. Self-acquisition of APLLs is often slow and unreliable, while DPLLs, a basic block diagram is shown in Figure 2.1, have faster locking speeds [17]. This is due to the basic operation of the analog low-pass filter and the analog multiplier in the phase detector (PD).

The low pass filter cannot extract the lower frequency within few input cycles since the narrow time windowing will destroy the information in the frequency domain (due to the time frequency resolution tradeoff). Same reasoning applies for the balanced modulator in the PD.

In contrast, a digital filter operation is based on a difference equation with convergence decided by the coefficients of the equation, and the PD operation

is related to the instant of sampling rather than to frequency comparison. This is why a DPLL can achieve locking within few cycles (see Chapter 3).

Hence DPLLs are tackled with concentration on sinusoidal DPLLs. The development of DPLLs started in the 1970's. The analysis of the positive-going zero-crossing sinusoidal DPLL was presented in 1980 using fixed point theorems [50, 51]. The second significant step in sinusoidal DPLLs was the digital tan-lock loop (DTL) in 1982 [13] that is based on the arctan phase detector which gave linear system equation. Since 1982 many efforts were made to improve the performance of DTL [52, 53, 54, 59]. In this book we emphasize a new DPLL that combines the two major approaches in the field: the approach of sinusoidal DPLL with fixed point analysis and the approach of DTL with the arctan phase detector. The main advantages of this DPLL, called the time delay digital tan-lock loop (TDTL), is the reduced complexity of the loop, wider lock range of the first-order loop and faster convergence speed under certain choice of the TDTL parameters.

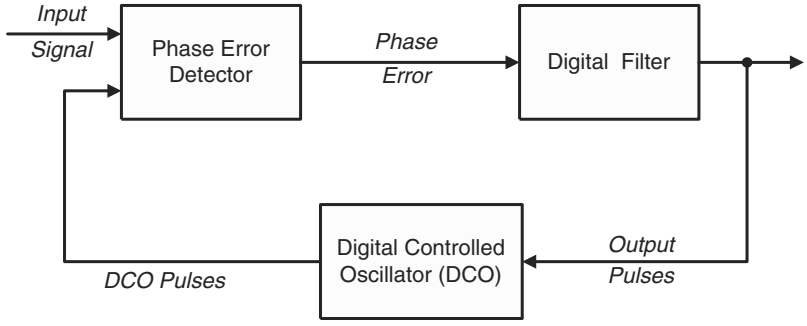


Figure 2.1: Basic block diagram of the digital phase locked loop.

2.2 Classification of DPLLs

Digital phase-locked loops can be classified into two major categories depending on the type of sampling process [12]

1. Uniform sampling DPLLs
2. Non-uniform sampling DPLLs

The DPLLs can be also classified according to the mechanization of the phase detector into five types as follows [12]

1. The flip-flop DPLL (FF-DPLL)

2. The Nyquist-rate DPLL (NR-DPLL)

3. The lead-lag DPLL (LL-DPLL), a.k.a binary-quantized DPLL (BQ-DPLL)

4. Exclusive-OR DPLL (XOR-DPLL)

5. Zero-crossing DPLL (ZC-DPLL)

Types 2 above belongs to uniform sampling, while the others belong to non-uniform sampling. A brief discussion of each type is given below.

Flip-flop DPLL

This kind of DPLLs was proposed in the literature by a number of authors [19], [20], [21] and [22].

In this type the phase detector is realized by a set-clear flip-flop and a counter as shown in Figure 2.2.

The sinusoidal input signal is converted into a square wave through an operational amplifier acting as a comparator. The output "Q" of the flip-flop is set to logic "1" on the positive-going edge of the comparator, and to logic "0" on the positive-going edge of the digital controlled oscillator (DCO). Hence the duration when Q is at level "1" will be proportional to phase error between the input signal and the DCO. This error is used to gate the counter clock which has a frequency of $2^M f_o$ where f_o is the center frequency of the DPLL and 2^M is the number of quantization levels of the phase error over period of 2π. The counter is zeroed and starts counting on the positive-going edge of the flip-flop waveform. The content of the counter, N_o, which is proportional to the phase error, is applied to the N-bit first-order digital filter which consists of proportional and accumulation paths. The output of the digital filter K controls the period of the DCO which consists basically of a programmable divide-by-K counter. It is the phase of the input signal that undergoes non-uniform sampling here rather than the amplitude.

Nyquist-rate DPLL

This DPLL was proposed in [23, 24] and subsequently developed by the works in [25], [26] and [27]. Nyquist sampling on the phase of the input signal rather than the amplitude was reported in [28]. In this DPLL the sinusoidal input signal is sampled *uniformly* at the Nyquist rate f_s and converted to N-bit digital signal by an analog-to-digital converter (ADC), then it is multiplied digitally by the DCO output $v(k)$ to form an error signal. This error signal is applied to

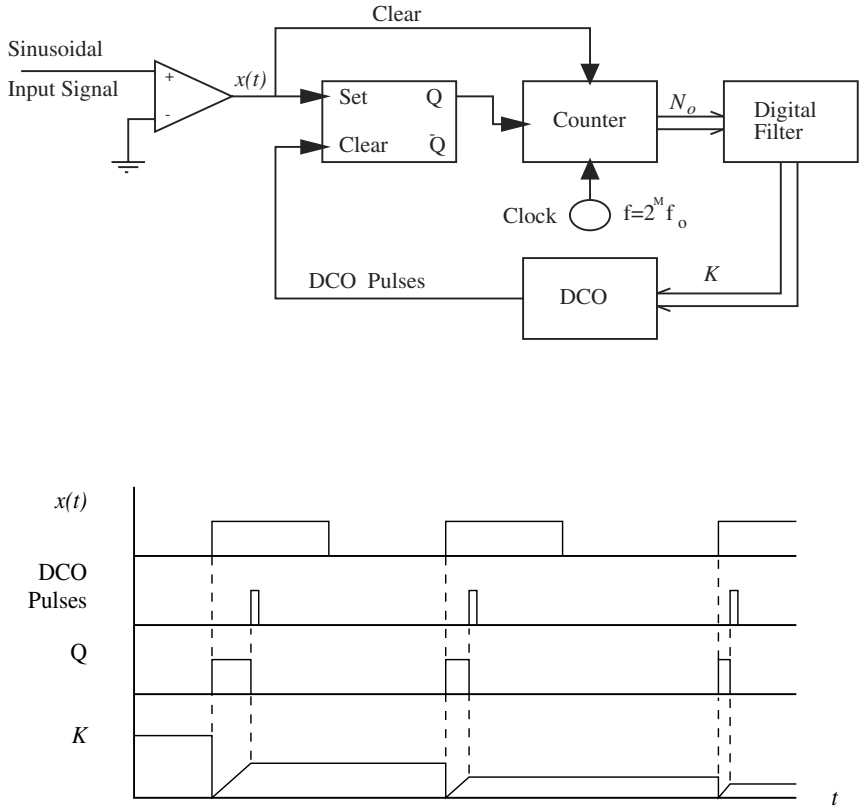


Figure 2.2: The flip-flop DPLL. Above: A block diagram. Below: Waveforms as a function of time.

N-bit digital filter whose output controls the period of the DCO as shown in Figure 2.3.

The DCO used in NR-DPLL is of algorithmic type [26]. It is constructed by utilizing the basic idea of the analog VCO. The analog VCO output can be given as in [29]

$$\mathrm{v}(t) = B\cos\left\{\omega_o t + G_o\int_{-\infty}^{t} y(\tau)d\tau\right\} \tag{2.1}$$

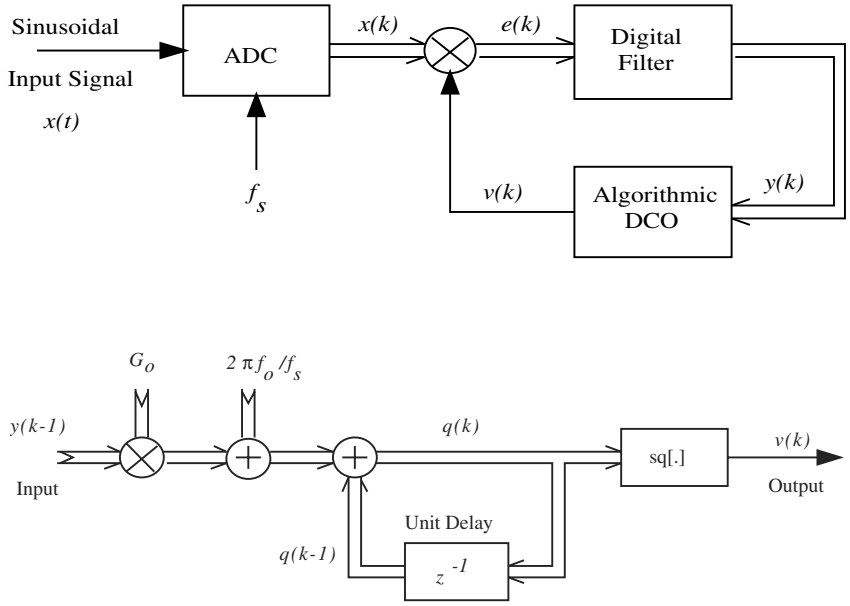


Figure 2.3: The Nyquist-rate DPLL. Above: A block diagram. Below: The algorithmic DCO.

where

$$\begin{aligned} \omega_o &= \text{center frequency of the VCO} \\ G_o &= \text{sensitivity of the VCO (rad/sec.volt)} \\ y(t) &= \text{input voltage} \end{aligned}$$

In the discrete time domain, (2.1) can be expressed as follows

$$\mathrm{v}(kT_s) = B\cos\left\{2\pi k f_o/f_s + G_o\sum_{n=0}^{k-1} y(n)\right\} \tag{2.2}$$

where $T_s = 1/f_s$ is the sampling period and $y(n) = y(nT_s)$. The sinusoidal function $\mathrm{v}(kT_s)$ is converted to a square wave $v(k)$ as follows

$$v(k) = \mathrm{sq}\left\{2\pi k f_o/f_s + G_o\sum_{n=0}^{k-1} y(n)\right\} \tag{2.3}$$

where

$$\begin{aligned} \mathrm{sq}(x) &= 1 \quad 0 \le x < \pi \\ &= -1 \quad \pi \le x < 2\pi \\ \mathrm{sq}(x) &= \mathrm{sq}(x + 2\pi) \end{aligned}$$

The direct implementation of (2.2) above is rather difficult due to the time-varying term $2\pi k f_o/f_s$. However, (2.2) can be written in the following form

$$v(k) = \mathrm{sq}\left[\sum_{n=0}^{k-1}\{2\pi k f_o/f_s + y(n)\}\right] = \mathrm{sq}[q(k)] \tag{2.4}$$

where

$$q(k) = \sum_{n=0}^{k-1}\{2\pi k f_o/f_s + y(n)\} \tag{2.5}$$

It can be shown that

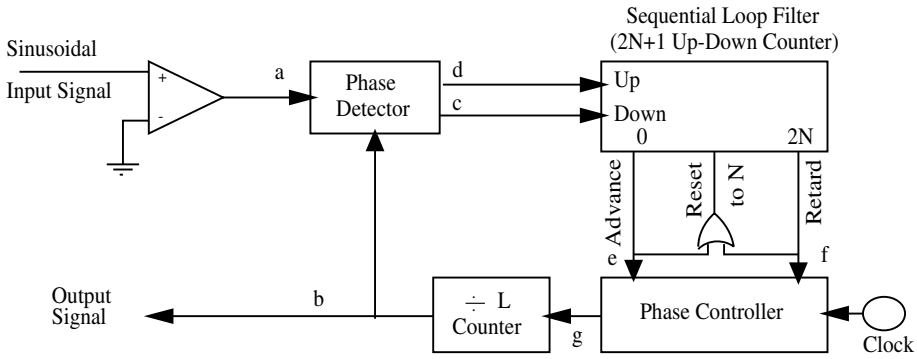
$$q(k) = q(k-1) + 2\pi f_o/f_s + G_o y(k-1) \tag{2.6}$$

Figure 2.3 shows the algorithmic DCO block diagram based on (2.3).

Lead-Lag DPLL

This type of DPLLs has been developed by the work in [30, 31] and extended in [32] to include a second-order sequential filter with memory. The LL-DPLL is characterized by the binary output of the phase detector that indicates whether the DCO waveform leads or lags the input signal. Due to this quantization it is often named "binary quantized DPLL". The input sinusoidal signal should be converted to a square wave by a comparator.

On the occurrence of a DCO pulse, either "lead" or "lag" terminal of the phase detector will give a pulse depending on the state of the input signal being "high" or "low", respectively, as shown in Figure 2.4. These pulses are applied to a special type of digital filters known as "sequential filter." The sequential filter deals with the input "lead" and "lag" pulses statistically; it observes them for a variable duration of time and gives a decision when a reliable limit is reached. Figure 2.4 shows that the sequential filter is composed of an up-down counter whose length is $2N + 1$. A pulse at the "lead" terminal causes the content of the counter to increase by 1, while the "lag" pulse behaves conversely. When the content of the counter reaches $2N$ or zero, the corresponding "Retard" (or: "Advance") output gives a pulse that resets the counter to "N" and triggers the phase controller. A "Retard" pulse causes the phase controller to delete one pulse



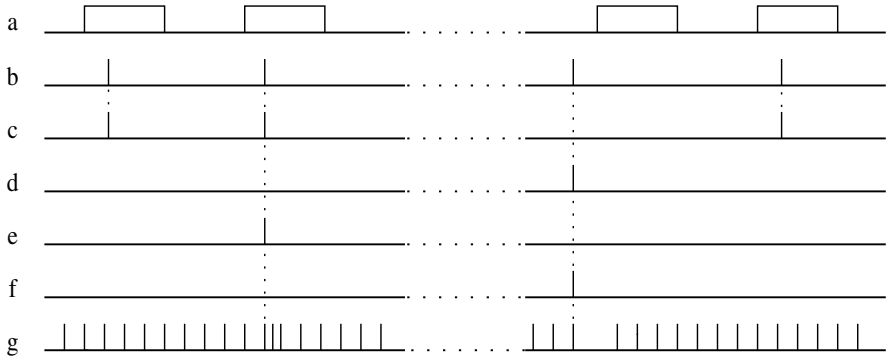


Figure 2.4: The lead-lag DPLL with associated waveforms.

from the clock pulse train that is applied to the divide-by-L counter, forcing the DCO phase to retard by $2\pi/L$, where L is the number of quantization levels of the period 2π. An "Advance pulse does the contrary.

When "lead" and "lag" pulses are equally probable, a case that indicates locking, the counter cycle has maximum duration. Other types of sequential filters exist like the N-before-M filter [12] and the variable reset random walk filter [32].

Exclusive-OR DPLL

Greer has utilized an exclusive-OR gate as a phase detector [17]. He used a K-counter as a digital filter and an increment-decrement (I/D) counter with a divide-by-N counter as a DCO. Figure 2.5 shows a block diagram of the Exclusive-OR DPLL.

The phase error detector (PED) compares the phase of the input signal, ϕ_{in}, with that of the loop output, ϕ_{out}, and gives an error signal ϕ_d defined as follows

$$\phi_d = K_o \, \phi_e \tag{2.7}$$

where K_o is the gain of the PED and $\phi_e = \phi_{in} - \phi_{out}$. The output of the PED can also be expressed as follows

$$\phi_d = (\%H - \%L)/100(\text{cycles}) \tag{2.8}$$

where $\%H$ and $\%L$ represent percentage "high" and "low" logic levels, respectively, during one cycle. Hence ϕ_d (in cycles) varies between +1 and -1. When $\phi_e = 1/4$ cycle ($\pi/2$ rad) then $\%H = \%L$ as shown in Figure 2.5-b, hence $\phi_d = 0 \equiv 2\pi \pmod{2\pi} = 1$ cycle, therefore $K_o = 4$.

The output of the phase detector controls the operation of the K-counter which consists of two divide-by-K counters, an up-counter and a down-counter, both triggered by a clock of rate Mf_o, where f_o is the center frequency and M is an integer. The output "C" of this counter, which is connected to the increment input (INR) of the I/D counter, generates a pulse when the K-counter ends an "up" cycle, while the "borrow" output B which is connected to the decrement input (DCR) generates a pulse on the end of a "down" cycle. A pulse applied to the "INR" input adds 1/2 cycle to the I/D output, while a pulse on the "DCR" input deletes 1/2 cycle.

The I/D counter clock runs at a frequency of $2Nf_o$, where N is the modulus of the divide-by-N counter that follows the I/D counter. The I/D counter is merely a divide-by-2 counter if no "INR" or "DCR" pulses are applied, hence its output frequency can be given by

$$\begin{aligned} F &= Nf_o + 1/2[K_o\phi_e M f_o/K] \ \text{(Hz)} \\ &= Nf_o + 2\phi_e M f_o/K \end{aligned} \tag{2.9}$$

The factor 1/2 above came from the fact that the I/D counter adds or deletes half a cycle when "INR" or "DCR" pulses are applied, respectively.

The output frequency can be expressed as

$$f_{out} = f_o + 2\phi_e M f_o/(KN) \quad \text{(Hz)} \tag{2.10}$$

Since ϕ_d varies between $+1$ and -1, ϕ_e varies between $+1/4$ and $-1/4$ cycles, hence lock range can be derived as follows

$$\begin{aligned} \Delta &= |f_{in} - f_o|_{\max} \\ &= |f_{out} - f_o|_{\max} \\ &= Mf_o/(2KN) \\ \text{lock range} &= 2\Delta = Mf_o/(KN) \end{aligned} \tag{2.11}$$

There exists a phase error between the input and the output signals even at locking, i.e. when $f_{out} = f_{in}$, which is given by [17]

$$\phi_e = KN(f_{in} - f_o)/(2Mf_o) \tag{2.12}$$

Figure 2.5-d clarifies this relationship.

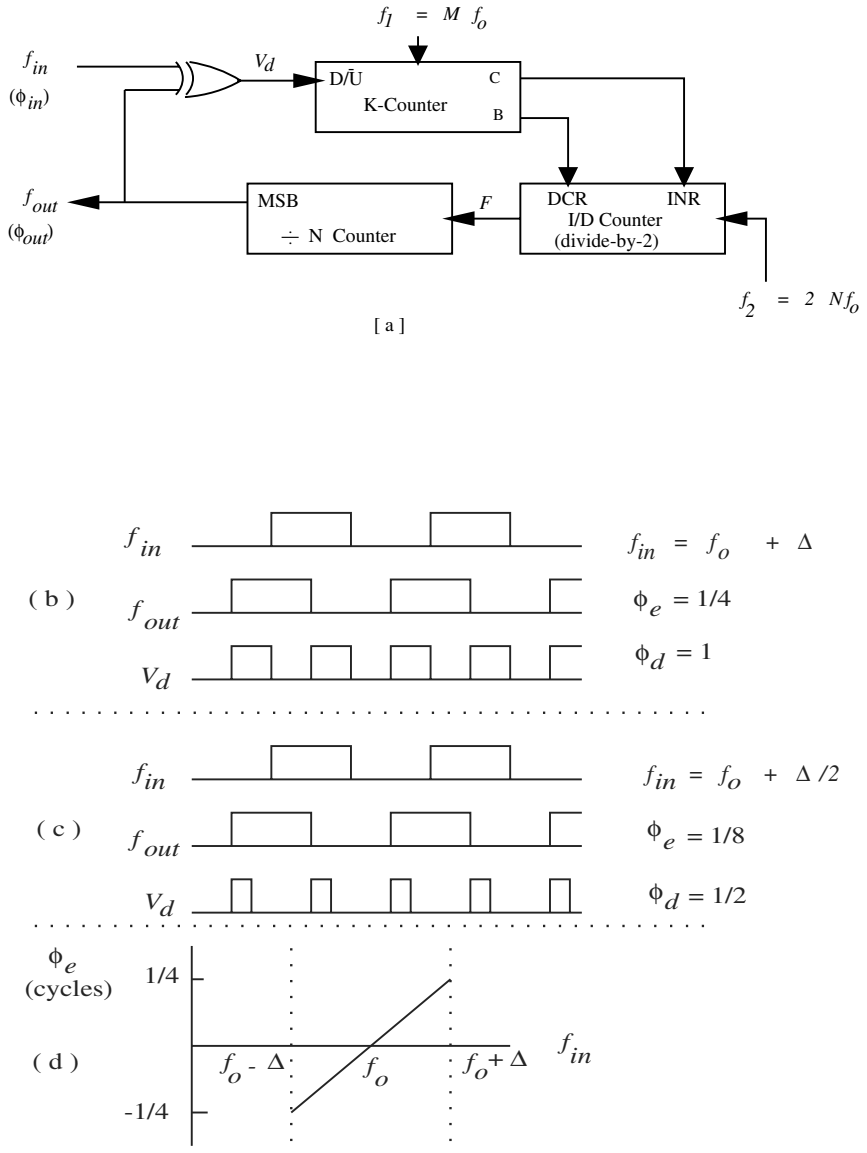


Figure 2.5: The Exclusive-OR DPLL with associated waveforms. (a) Block diagram. (b) Waveforms at $f_{in} = f_o + \Delta$. (c) Waveforms at $f_{in} = f_o + \Delta/2$. (d) Transfer function at lock.

Zero-Crossing DPLL

This type of DPLLs accepts sinusoidal signals and samples the input signal at or near zero crossings, hence the name zero-crossing DPLL (ZC-DPLL).

There are two variations of ZC-DPLLs. The first, named $ZC_1 - DPLL$, samples only on the positive-going zero crossings, while the other type, $ZC_2 - DPLL$, samples on both positive and negative-going zero crossings. The first type is the most important type of DPLLs since it is the simplest to implement, the easiest to model, and its operation and performance are indicative of the general behavior of any DPLL [12]. Although $ZC_2 - DPLL$ locks faster, it has additional design complications over $ZC_1 - DPLL$ [12, 111], hence the latter dominated.

$ZC_2 - DPLL$ has been proposed first in [33] and developed later as discussed in [34] and [35]. $ZC_1 - DPLL$ has been developed by the work in [36, 37, 38, 39, 40, 41, 42]. The systematic statistical analysis of $ZC_1 - DPLL$ is provided in [43] where it presents a numerical solution to the Chapman-Kolmogorov equation. Other studies on this have also been presented in the literature [44, 45, 46, 47, 48, 49, 50, 51]. In 1982 a new classification was imposed on DPLLs by the advent of the digital tanlock loop (DTL) [13]. $ZC_1 - DPLL$ and $ZC_2 - DPLL$ were given the name "sinusoidal ZC-DPLL" or simply "sinusoidal DPLL" [13], based on the phase detection technique. DTL is a new type of $ZC_1 - DPLLs$ that has distinguished phase detection mechanism and significant advantages over other types of DPLLs. Many efforts have been made to improve the characteristics of DTL and its application in communication systems [52, 53, 59].

A brief description of the sinusoidal $ZC_1 - DPLL$ and DTL is given below.

Sinusoidal $ZC_1 - DPLL$

Figure 2.6 shows the block diagram of sinusoidal $ZC_1 - DPLL$ with the associated waveforms. Here the function of phase detection is merged with that of non-uniform sampling since the instant of sampling determines the phase error [38, 50]. The main parts of this DPLL are explained below.

The N-bit Digital Filter

This filter modifies the analog-to-digital converter (ADC) samples, which are applied to the DCO, in such a way that leads the phase error to reach a constant value and hence locking occurs. The digital filter consists of proportional and accumulation paths.

The order of the digital filter represents the order of its difference equation, hence the n^{th}-order digital filter can be described in the z-domain by the

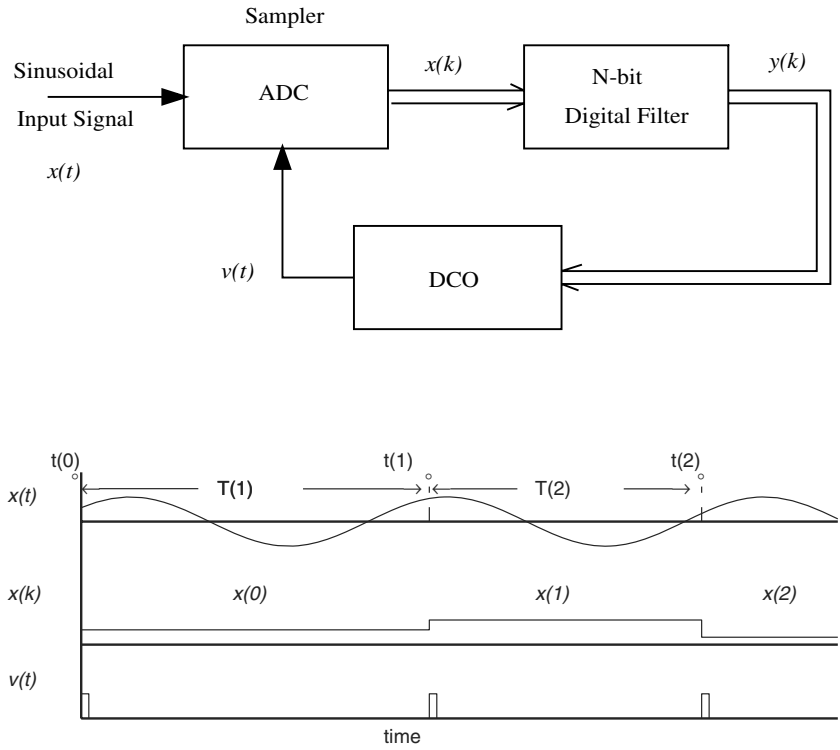


Figure 2.6: The Sinusoidal $ZC_1 - DPLL$ with associated waveforms.

following transfer function [39]

$$D(z) = \kappa \frac{(z + c_1)(z + c_2)...(z + c_n)}{(z + p_1)(z + p_2)...(z + p_n)} \tag{2.13}$$

Since the present value of the phase error depends on the previous value, the order of the loop equals the order of the digital filter plus one. Hence in the first-order loop the digital filter is just a proportional path, while the second-order loop utilizes a first-order digital filter with the following transfer function

$$D(z) = \kappa(z + c_1)/(z + p_1) \tag{2.14}$$

For the second-order sinusoidal $ZC_1 - DPLL$ to lock on zero phase error, p_1 must equal -1 [39], hence (2.14) may be written in a more convenient form as follows

$$D(z) = G_1 + G_2/(1 - z^{-1}) \tag{2.15}$$

which gives in the time domain the following input-output relation

$$y(n) = G_1\, x(n) + G_2 \sum_{k=0}^{n} x(k) \tag{2.16}$$

where $x(k)$ and $y(k)$ are the discrete input and output signals, respectively.

The Digital Controlled Oscillator (DCO)

The digital controlled oscillator consists of a programmable counter, a binary subtracter, and zero detector. Figure 2.7 shows a block diagram of DCO with associated waveforms. Subtraction is performed using a 2's complementer and a full adder. The counter content is decremented by one on the occurrence of each clock pulse. When it reaches zero, the counter generates a pulse at the output. This pulse is used to load the counter with the binary number $M - K$ where M is a constant number and K is the input number. The number M decides the DCO free-running frequency f_o when the input number K is zero as follows

$$f_o = f_c/M \tag{2.17}$$

where f_c is the frequency of the counter clock. The period between the $(k-1)^{th}$ and the k^{th} pulses is given by

$$T(k) = (M - K)\, T_c \tag{2.18}$$

where $T_c = 1/f_c$.

The Phase Equation

The input signal $x(t)$ is assumed to be in the form

$$x(t) = A\ \sin\{\omega_o t + \theta(t)\} + n(t) \tag{2.19}$$

where A is the signal amplitude, $\omega_o = 2\pi f_o$, $\theta(t)$ is the information bearing phase, and $n(t)$ is Gaussian additive noise. For a frequency step input $\theta(t)$ is given by

$$\theta(t) = (\omega - \omega_o)t + \theta_o \tag{2.20}$$

where θ_o is a phase constant and ω is the input frequency. Under such condition the (nonlinear) difference equations representing the first-order loop (with

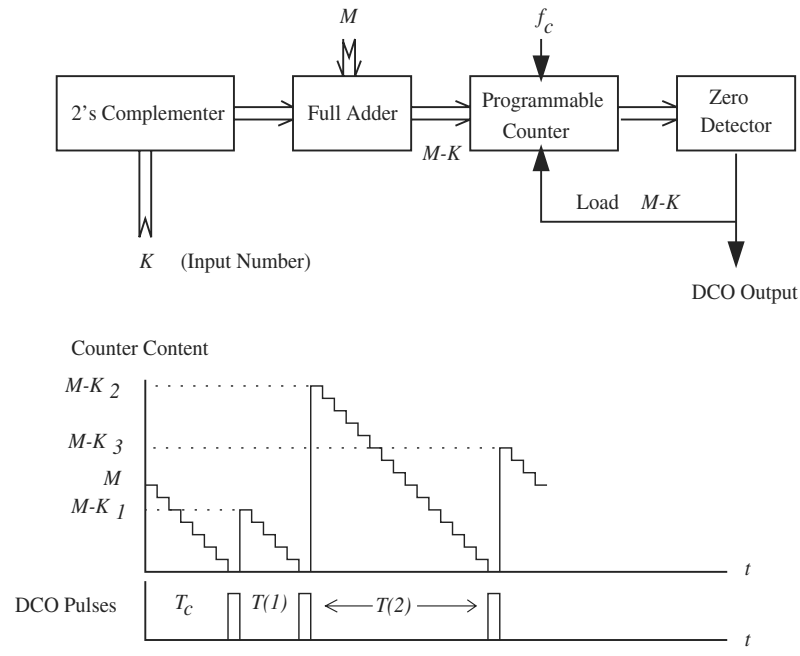


Figure 2.7: The digital controlled oscillator with associated waveforms.

$D(z) = G_1$) and the second-order loop (with $D(z) = G_1 + G_2 z/(z-1)$) can be respectively given by [50, 51]

$$\phi(k+1) = \phi(k) - K_1^{'} \sin\{\phi(k)\} - K_2^{'} n(k) + \Lambda_o \tag{2.21}$$

and

$$\begin{aligned} \phi(k+1) &= 2\phi(k) - \phi(k-1) + K_1^{'} \sin\{\phi(k)\} \\ &\quad -K_2^{'} n(k) - r[K_1^{'} \sin\{\phi(k)\} + K_2^{'} n(k)] \end{aligned} \tag{2.22}$$

where $\phi(k)$ is the phase error at the instant k, $K_1^{'} = \omega G1\ A$, $K_2 = \omega G_1$, $\Lambda_o = 2\pi(\omega - \omega_o)/\omega_o$, and $r = 1 + G_2/G_1$. From these equations it can be shown that the noise-free steady-state phase error of the first-order loop is given by

$$\phi_{ss} = \sin^{-1}(\Lambda_o / K_1^{'}) \tag{2.23}$$

while the second-order loop locks on zero phase error.

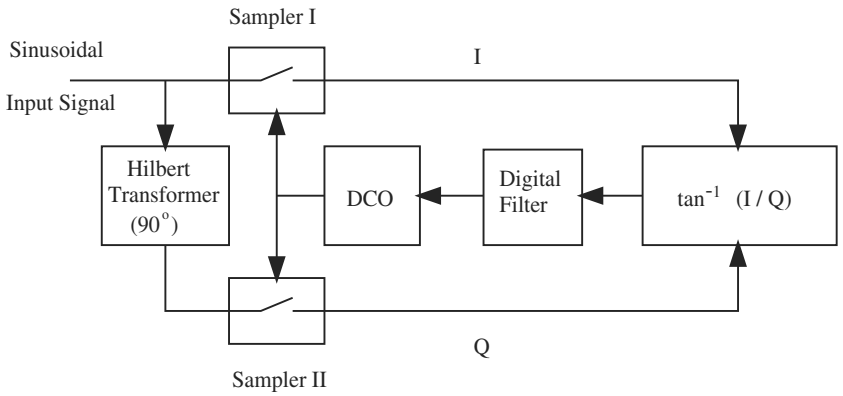


Figure 2.8: Structure of the digital tanlock loop.

Although sinusoidal DPLL has many advantages over other types of DPLLs [12], it has the shortcomings of sensitivity to the variations in the input signal power and rather limited lock range. The DTL explained below has solved these problems.

The Digital Tanlock Loop (DTL)

This DPLL was introduced in [13]. Figure 2.8 shows a block diagram of DTL. It is composed of 90^o phase shifter, two samplers, a phase error detector, a digital loop filter, and a digital controlled oscillator (DCO). Sampler I takes a sample I of the incoming signal, and sampler II takes a sample Q of the phase-shifted version of the incoming signal simultaneously. The phase error, which is determined by the sampling instant, is extracted by the $\tan^{-1}$ function at the phase error detector. This phase error is modified by the digital filter whose output controls the period of the digital controlled oscillator (DCO). This technique in the phase detection along with the use of a Hilbert transformer led to a linear phase difference equation.

The noise-free difference equations of the first and second-order DTLs are given respectively by [13]

$$\phi(k+1) = (1 - K_1^{'})\phi(k) + \Lambda_o \tag{2.24}$$

and

$$\phi(k+2) = (2 - rK_1^{'})\phi(k+1) + (K_1^{'} - 1)\phi(k) \tag{2.25}$$

where all symbols are defined in the paragraph of sinusoidal $\mathrm{ZC}_1 - \mathrm{DPLL}$.

The steady-state phase error of the first-order DTL is

$$\phi_{ss} = \Lambda_o / K_1^{'} \tag{2.26}$$

and the second-order DTL locks on zero phase error. Due to dividing the input signal by its phase-shifted version at the phase error detector, DTL noise-free performance is independent of the signal amplitude A, hence under noise-free condition DTL is insensitive to the variations in signal power. The first-order DTL has wider lock range than the sinusoidal DPLL.

The analysis of sinusoidal DPLL is nonlinear and based on "fixed point theorems" [50, 51], while the analysis of the DTL is linear. Our work in this book combines the two major approaches in the field: the approach of sinusoidal DPLL built on fixed point analysis and the approach of tanlock based on the arctan phase detection. Our main objective is to reduce the complicated structure of DTL while preserving its advantages.

2.3 Conclusions

In this chapter we have presented a survey of digital phase-locked loops (DPLLs). The survey included the major classification of DPLLs according to the sampling scheme where they are classified as uniform and non-uniform sampling DPLLs. Further classification according to the phase detection scheme was also considered. The main parts in each class are clarified.

It has been shown that the most important kind of DPLLs is the non-uniform sampling sinusoidal zero-crossing DPLL (ZC-DPLL). Hence we will concentrate on this kind of DPLLs in this book. Developments in this respect are presented. Two major approaches exist in this field: the original approach of sinusoidal DPLL built on fixed point analysis and the approach of tanlock phase detection. In this book we will present a combination of the above two approaches that will give many advantages over the existing types of DPLLs.