Chapter 2
Analog Properties of Multi-Gate MOSFETs

This chapter reviews the main multi-gate device characteristics relevant for analog and mixed-signal circuit design. The objective is to close the link from technology and integration aspects to analog device performance. The associated trade-offs are outlined. The introduction of three-dimensional multi-gate devices with high-k/metal gate stack represents "revolutionary" changes in CMOS technology. Therefore a close insight to analog device behavior serves as basis for the technology oriented circuit design issues addressed later.

First an example for a recent FinFET technology is introduced. Then DC, small signal, RF, noise and matching performance is discussed and compared to similar planar devices. Finally charge-trapping and self-heating are covered as example for novel technology related device effects.
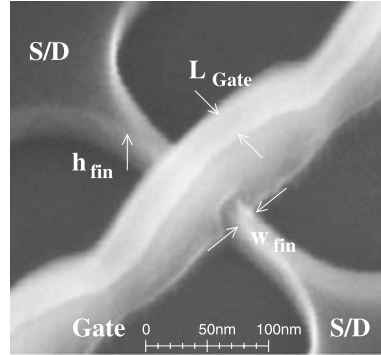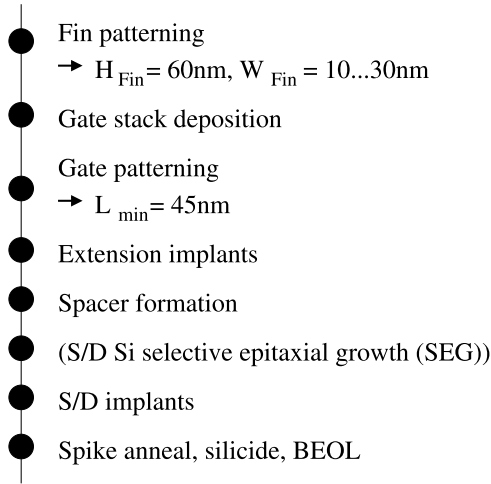
2.1 Introduction to Recent FinFET Technology

All measurement and simulation results shown here are based on recent low-power multi-gate CMOS technologies as presented in [6] and [54]. Technology details for the planar reference devices are given in [55] and [56].

The basic FinFET process flow is illustrated in Fig. 2.1. Fins are patterned in a 60 nm high undoped[1] silicon layer on standard 200 mm or 300 mm SOI wafers. Dedicated optical proximity correction (OPC) allows to process fin widths w_{fin} down to 10 nm. For circuit evaluation in this work w_{fin} typically is chosen around 20 nm...30 nm. The effective channel width per fin in these triple gate devices is $2h_{fin} + w_{fin} \approx 0.14$ μm. Taking the fin pitch of 200 nm into account, the area efficiency is reduced compared to planar. However, several techniques to reduce the fin pitch and improve the area efficiency have already been proposed, e.g. double patterning [57]. HfSiON is deposited as high-k dielectric, yielding EOT values of about 1.6 nm. For comparison also SiON reference devices with EOT of 1.9 nm

---

[1]Undoped means doping levels below 10^{15} cm^{-3}.

- Fin patterning
  → H_{Fin} = 60nm, W_{Fin} = 10...30nm
- Gate stack deposition
- Gate patterning
  → L_{min} = 45nm
- Extension implants
- Spacer formation
- (S/D Si selective epitaxial growth (SEG))
- S/D implants
- Spike anneal, silicide, BEOL

Fig. 2.1 FinFET process flow and SEM picture of single fin device after gate patterning

are processed. TiN is used as gate electrode material. Due to the undoped fins midgap workfunction is required for symmetric nFET and pFET threshold voltages. To achieve mid-gap workfunction on both dielectrics the TiN thickness is adjusted between 5 nm and 10 nm. If needed, additional capping and V_T adjust layer(s) are deposited below and on top of the metal gate. The gate stack is completed with a poly silicon layer which is finally silicided to reduce the contact resistance. A concrete example for a high-k/metal gate stack is shown later in this chapter. Additional gate etching enables nominal gate lengths of 45 nm [54] and 65 nm [6]. After spacer formation the fin width is optionally increased by selective epitaxial growth. Then source/drain regions are implanted vertically or 45° tilted. Further process steps include annealing, silicidation and finally copper metallization (BEOL).

2.2 DC Characteristics

It was shown in Chap. 1 that the electrostatic integrity, i.e. the short-channel behavior is determined by the relation of fin thickness to channel length at given EOT. A rule of thumb to keep short channel effects under control is that the fin width w_{fin} should not exceed 2/3 of the minimum channel length [31, 32]. For the devices considered here this requirements is always fulfilled. The measured transfer characteristics of a n-type FinFET featuring minimum gate length L_{min} = 45 nm shown in Fig. 2.2 proves that excellent short channel behavior is achievable with proper engineered FinFETs. Very low DIBL effect (<25 mV) and close to ideal sub-threshold slope (≈70 mV/Dec) are obtained, see Table 2.1. The well controlled short channel effects enable very low leakage currents (measured at V_{GS} = 0 V and $V_{DS} = V_{DD}$ = 1.0 V), whereas the on-currents (measured at $V_{GS} = V_{DS} = V_{DD}$)
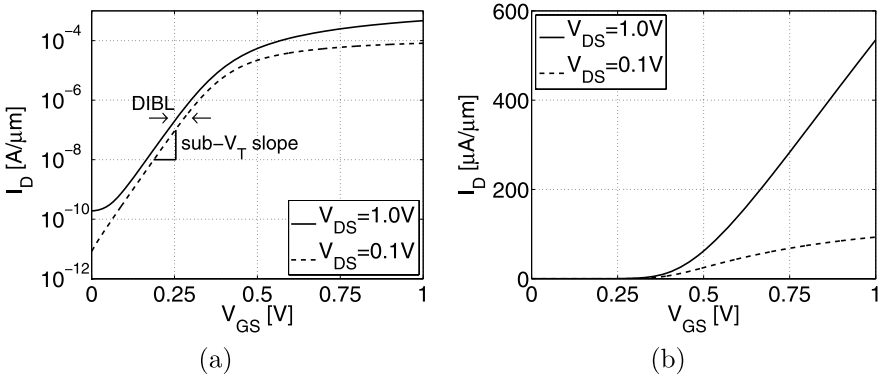
Fig. 2.2 Measured transfer characteristic in saturation (*full lines*) and linear (*dashed lines*) regime of n-type FinFET with $L_{gate} = 45$ nm

Table 2.1 Digital performance of FinFET with $L_{gate} = 45$ nm and $V_{DD} = 1.0$ V

	nFET	pFET
I_{ON} [µA]	534	452
I_{OFF} [nA]	0.31	0.42
I_{GATE} [nA]	0.09	0.07
V_T [V]	0.35	−0.34
DIBL [mV]	24	26
Sub-V_T slope [mV/Dec]	69	73

Fig. 2.3 Measured output characteristic of n-type FinFET with $L_{gate} = 45$ nm for V_{GS} from 0.2 to 1.0 V
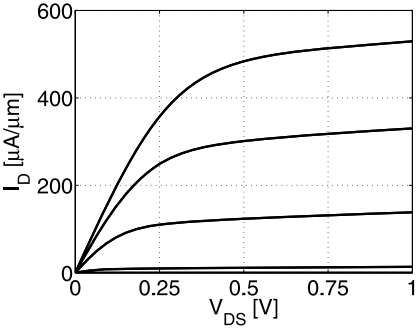
meet the ITRS targets for low standby power devices. The off-currents in this example are not limited by sub-threshold leakage but by gate-induced drain leakage. Gate leakage currents are suppressed by the high-k dielectric. The digital device characteristics is summarized in Table 2.1, nFET and pFET feature almost the same performance. The high pFET on-current results from the (110) surface orientation of the fin sidewalls with high hole mobility. The reduced short channel effects affect also the output characteristics I_D−V_{DS} shown in Fig. 2.3: in contrast to aggressively
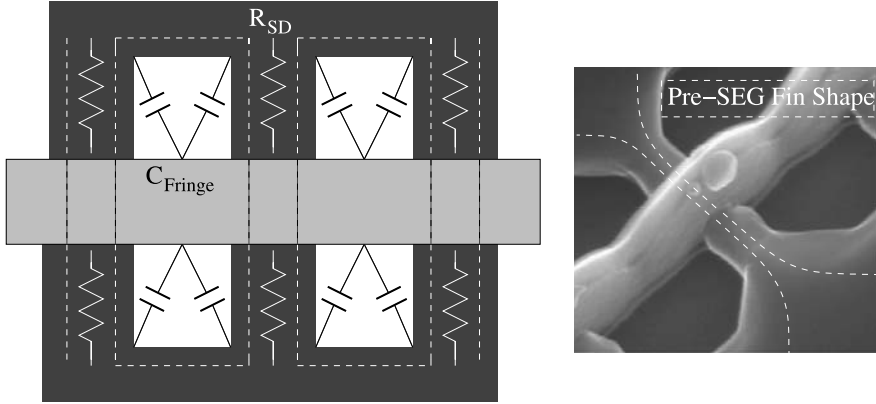
Fig. 2.4 Schematic view and SEM picture of FinFET before and after SEG including parasitics

scaled planar bulk CMOS technologies [58] the slope of the drain current in saturation is not increased by pronounced DIBL effect.

Another FinFET specific characteristic is visible in the linear I_D–V_{GS} plot of Fig. 2.2(b). The slope of the drain current in saturation flattens form quadratic to linear behavior at lower V_{GS} values than usually observed in planar bulk devices. This effect can be explained by high parasitic source/drain series resistances R_{SD} in the narrow fins which connect the channel to the source/drain contact landing pads, see Fig. 2.1.

Wider fins are no viable solution for this issue because short-channel and leakage requirements enforce a certain L_{gate}/w_{fin} ratio. Besides different mobility enhancement techniques one approach to improve the drive current therefore is to widen the fins outside of the gate, e.g. by selective epitaxial growth (SEG). SEG as illustrated in Fig. 2.4 has been used to decrease the source/drain resistances yielding higher drive currents [59]. However, the widening of the fins results in increased parasitic fringe capacitances which affect the RF performance. Nevertheless, it has been shown recently that despite of the additional parasitic capacitances FinFETs can achieve performance advantages over planar bulk at 22 nm node dimensions [60].

2.3 Analog and RF Characteristics

The most important analog and RF device figures-of-merit determining circuit resolution, speed and power consumption are the small signal parameters, noise and matching behavior. As starting point for analog and RF circuit design typically a simple linear equivalent circuit model is used [61]. The transistor behavior is linearized in a certain bias point and modeled by linear sources, resistors and capacitances, for more details see [62]. The slopes in the linearized approximation are called small signal parameters.

2.3.1 Small Signal Parameters

The relevant parameters regarding the analog performance are the transconductance g_m, the output conductance g_{ds} and the intrinsic gain g_m/g_{ds}. The transconductance describes how efficient a small voltage signal at the transistor gate is converted into a drain current signal. On circuit level the available g_m limits e.g. the bandwidth of operational amplifiers. Figure 2.5(a) shows measured gate length dependence of g_m for n-type FinFET and planar reference devices at typical analog bias conditions ($V_{GS} = V_T + 200$ mV and $V_{DS} = 1$ V). The FinFET g_m is slightly lower compared to the planar reference mainly due to the high parasitic source/drain resistances [63]. The situation gets worse for shorter channel lengths and increasing overdrive voltage $V_{GS} - V_T$.

The output conductance g_{ds} describes the quality of the device as constant current source. In modern planar CMOS technologies g_{ds} is not only determined by the channel length modulation but furthermore degraded for different reasons: pronounced DIBL effects cause a significant V_T dependence on V_{DS} which again leads to an enhanced (non-linear) drain current dependence on V_{DS}, visible as degraded output conductance. In order to keep short-channel-effects at tolerable levels typically strong pocket or HALO implants are necessary in planar bulk devices. These implants close to the source/drain extensions are intended to confine the source/drain field penetration. Implicitly an additional barrier is introduced at the drain end of the channel which can be modulated with the drain source bias. Especially at longer gate lengths this barrier results in a large residual DIBL-like effect yielding again degraded g_{ds} values [64]. The effect is sometimes called drain induced threshold shift to distinguish from DIBL because the effect is related to the drain barrier. This g_{ds} degradation for long channel devices strongly affects analog circuit design in scaled CMOS, since the efficiency of the common way to enhance output resistance is partly lost.

In fully-depleted FinFET devices the main contributors to the g_{ds} degradation are no concern: due to the enhanced electrostatic integrity short channel effects
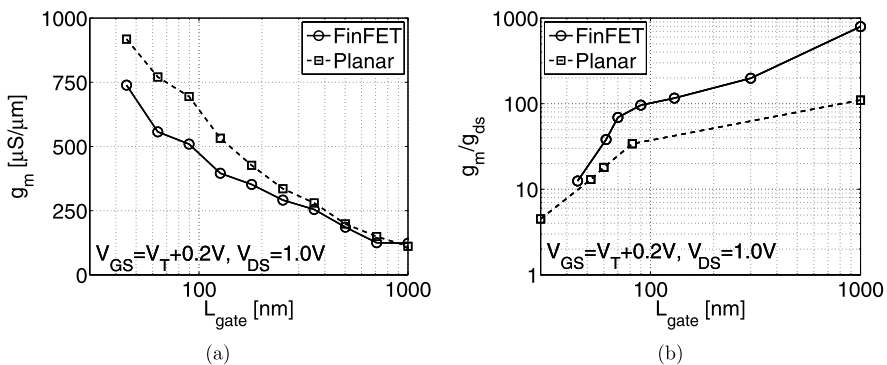
Fig. 2.5 Measured g_m (**a**) and intrinsic gain g_m/g_{ds} (**b**) of n-type planar and FinFET devices for varying L_{gate}

are well controlled by the device structure itself, the fins are left undoped and no HALO implants are necessary. For a fair assessment not the g_{ds} but the intrinsic gain g_m/g_{ds} is considered. The intrinsic gain represents the maximum voltage gain achievable with a single device. Figure 2.5(b) compares FinFET g_m/g_{ds} gate length dependence to planar reference devices at typical analog bias points. Even at short gate lengths the FinFET features improved gain, although its g_m is slightly lower. At longer gate lengths the difference accounts approximately for a factor 3 to 9. Obviously the reason for the high intrinsic gain of FinFETs is the very low output conductance.

The drain current efficiency is defined as ratio of g_m/I_D and limits the achievable bandwidth at given current (power) consumption on circuit level. Figure 2.6(a) shows the efficiency of n-type planar and FinFET device with 90 nm gate length

(a)

(b)

(c)
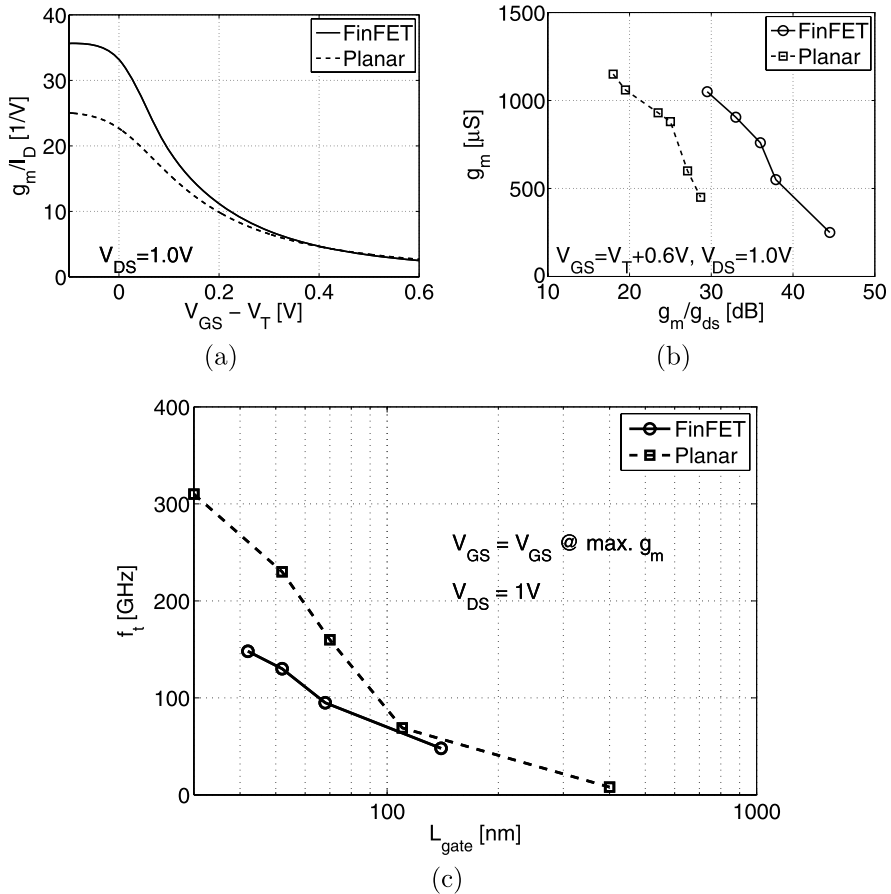
Fig. 2.6 Measured efficiency g_m/I_D of n-type planar and FinFET device with 90 nm gate length (**a**), g_m vs g_m/g_{ds} trade-off (**b**) and transit frequency f_t (**c**) of planar and FinFET devices for varying L_{gate}

versus gate overdrive. Below V_T the FinFET efficiency is significantly improved due to the reduced short channel effects and the corresponding steep sub-V_T slope. At typical low-power analog bias points with moderate overdrive voltage the Fin-FET is still more efficient, whereas the large series resistances degrade g_m/I_D at high overdrive. The gain versus bandwidth (g_m/g_{ds} versus g_m) trade-off is another important criterion for analog device performance. Figure 2.6(b) compares FinFET and planar devices at high gate overdrive, typically used in high speed applications. Similar to the "low-power" bias points planar devices offer higher maximum g_m, however at much worse gain values. From analog perspective, the high intrinsic gain is a strong argument to use multi-gate devices in future technology nodes, as it overcomes one of the most critical scaling issues in planar bulk CMOS. A quantitative estimation of the resulting benefits for analog circuits is presented later.

For RF circuits the transit frequency f_t and the maximum oscillation frequency f_{max} are key figures-of-merit, defining the unity gain frequencies for current and power respectively. Both quantities relate the achievable transconductance to "parasitics" as gate-source and gate-drain capacitances C_{GS}, C_{GD}. In case of f_{max} also the gate resistance R_G is considered. Figure 2.6(c) shows measured f_t for FinFET and planar reference at maximum g_m. Compared to planar, the f_t of the FinFETs is significantly reduced, mainly due to the higher parasitics: the large source drain resistances R_{SD} limit g_m as shown above and additional fringing capacitances from source drain contact landing pads to the gate contribute to C_{GS} and C_{GD}. The usage of SEG is a limited solution in this case, because any decrease in R_{SD} achieved with wider fins is traded against higher fringing capacitance, see Fig. 2.4. Regarding f_{max} the situation is similar. Nevertheless the currently achievable f_t and f_{max} values well above 100 GHz allow competitive RF circuits in the sub 10 GHz regime as shown later.

The introduction of high-k dielectrics eventually leads to an additional decrease of f_{max} caused by an higher vertical gate resistance. Without careful gate stack engineering the vertical gate resistance can be degraded due to the large number of different interfaces typically present in high-k/metal gate stacks. Figure 2.7(a) illustrates an example containing a SiON interface layer, the main HfSiON high-k dielectric, TiN metal gate electrode, V_T adjust capping layer(s), poly-Si capping and finally the silicide. Of course higher gate resistances affect also noise performance in addition to f_{max}. However this potential issue is not FinFET specific but may occur in any future CMOS technology containing high-k materials.

2.3.2 Noise Performance

Thermal and flicker noise are two important noise sources relevant for analog and RF design. The most significant thermal noise source in saturation is the channel. The spectral noise density is given by g_m [45] and consequently independent of device architecture and materials. The increased source drain resistance of the FinFET
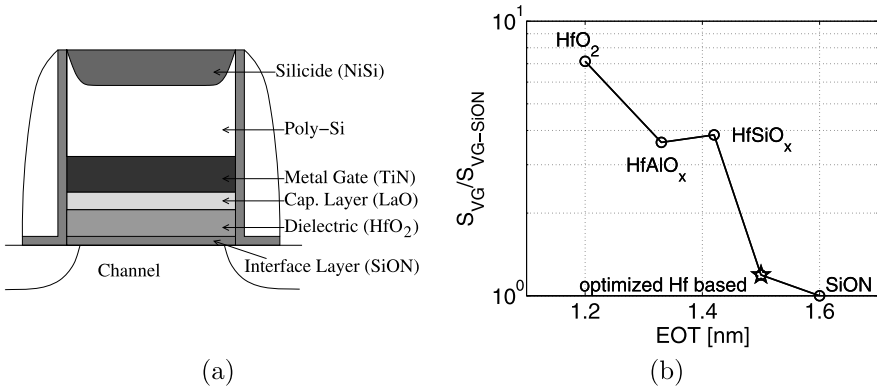
Fig. 2.7 Schematic cross-section of high-k/metal gate stack with exemplary materials (**a**) and relative flicker noise vs EOT trade-off for different dielectric materials (**b**) [65]

may yield slightly higher noise. In contrast to thermal noise, flicker noise strongly depends on technology as explained in Chap. 1. Especially the surface and interface quality is crucial for the flicker noise performance.

Consequently the introduction of high-k dielectrics is a potential source for degraded flicker noise performance due to a high defect density in the high-k dielectric bulk and an increased interface state density [65]. Since flicker noise is very sensitive to many parameters such as thickness and material of interfacial layer and high-k dielectric [46, 47, 66], careful tuning and gate stack engineering is necessary. Exploiting the technology trade-offs combined with lots of process optimization recently a planar bulk CMOS technology featuring high-k/metal gate has been presented [67], achieving competitive flicker noise performance compared to SiON. It is noteworthy that this performance is still worse than what can be achieved with "traditional" SiO_2. Particularly with respect to further scaling of CMOS and the introduction of further novel dielectrics there will be still a material related trade-off between EOT scaling and noise performance as shown in Fig. 2.7(b).

Regarding the FinFET structure there are two potential origins for degraded surface quality and increased flicker noise: the fin sidewalls, which compose about 80% of the channel cross-section, typically feature a (110) crystal orientation which is known to have worse flicker noise behavior [68]. In addition the vertical etch of the fin sidewalls is challenging. Compared to the top surface the roughness of the sidewalls typically is increased. For this reason annealing steps are required to smooth the sidewalls and to achieve sufficient surface quality [31].

Figure 2.8 compares measured spectral noise density of FinFET and planar devices for varying gate overdrive at 1 Hz. The planar reference devices in 32 nm low-power CMOS feature hafnium based high-k dielectric and metal gates [67]. No significant degradation is observed for the FinFET devices with HfSiON dielectric and TiN gate electrode. Both, FinFET and planar are close to ITRS targets for analog, mixed-signal and RF technologies [69].
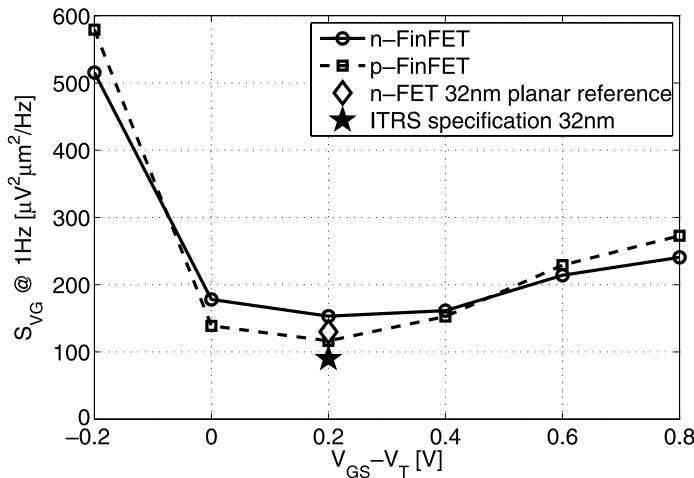
Fig. 2.8 Comparison of measured spectral noise density of FinFET and planar devices for varying gate overdrive at 1 Hz

2.4 Matching Behavior

As shown in Chap. 1 parameter mismatch limits resolution, area and power of analog and mixed-signal circuits. In today's CMOS technologies typically the V_T mismatch induced by random doping fluctuations is dominant, however other effects such as line-edge roughness start to limit scaling of mismatch with EOT according to (1.9).

The introduction of high-k dielectrics impacts matching in a similar way as flicker noise, since both phenomena are related to statistically distributed states and charges. Hence, high-k dielectrics are potential sources for a degradation of matching performance. Pre-existing states and fixed charges at the interface and in the dielectric are randomly distributed and cause local V_T variations comparable random dopant fluctuation. Again, process optimization and dedicated gate stack engineering are required to achieve sufficient matching. On the other side high-k/metal gate offers ways to improve or at least maintain matching performance. The effect of poly depletion (and its variation) is eliminated by the metal gate electrode. Additionally high-k enables scaling of EOT without gate-leakage problems. This EOT scaling enables improved matching constants. Recent 32 nm CMOS technologies prove that high-k is no issue with respect to V_T matching [67].

Compared to planar bulk CMOS the fully depleted FinFET structure offers major advantages: the fin, i.e. the channel region is undoped and the threshold voltage is adjusted by the workfunction of the gate electrode. Since the V_T matching constant shows a square root dependence on the doping level, FinFETs are expected to feature advantageous matching behavior. However, other FinFET specific effects related to fin shape and surface roughness have to be considered with respect to matching [70, 71]. Especially narrow fin devices are affected as illustrated in Fig. 2.9.
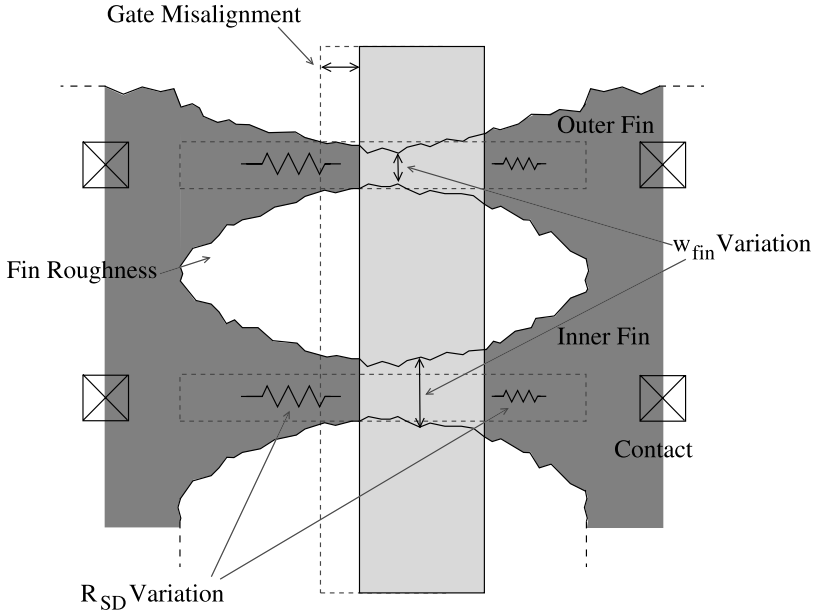
Fig. 2.9 FinFET specific mismatch effects related to fin shape, surface roughness and mask alignment within a multiple fin device

- *Surface roughness*: as explained above, the surface quality of the fin sidewalls is critical. Increased defect and interface state density results in degraded V_T matching.
- *Fin width variations*: the etching of the fins leads to a more or less pronounced broadening of the fin shape in direction to the source and drain landing pads. Particularly in short channel devices this effect has to be considered. Process related, the broadening varies and leads to variations in effective channel width.
- *R_{SD} variations*: (asymmetric) variations in fin width outside of the gate are equal to variations of the source drain series resistances, affecting I_D, g_m etc.
- *Difference between inner and outer fins*: The fin shape of inner fins within a multiple fin device and the two outer fins varies due to the different surrounding: obviously the broadening of the outer fins is different. Lithography requirements enforce different OPC rules for inner and outer fins, which induces additional mismatch.
- *Gate misalignment*: Due to misalignment of masks used in litho process the gate is never perfectly centered between source drain landing pads, resulting in an asymmetric fin shape covered by the gate. Consequently the broadening of the fin is more pronounced on one side of the channel. Since the fin width determines the electrostatics of the device, the asymmetry affects V_T. The amount of V_T shift depends on the direction of misalignment, where the device is more sensitive on the source side.
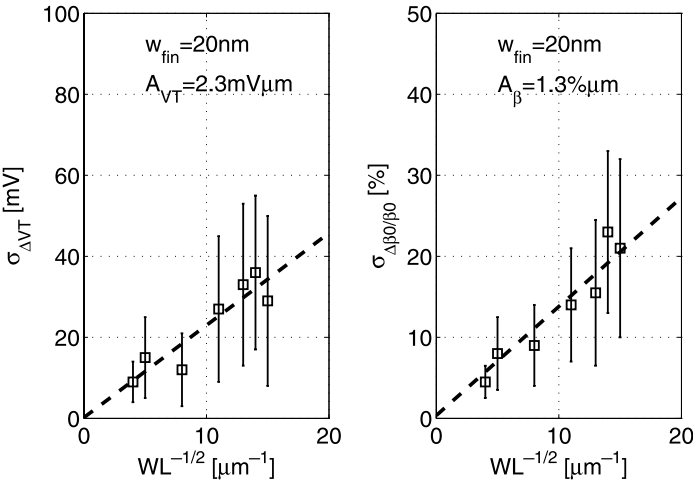
Fig. 2.10 Pelgrom plots of n-type FinFET with 20 nm fin width for V_T and β matching

Table 2.2 Measured matching constants for n- and p-type FinFET with 10 nm and 20 nm fin width

	nFinFET		pFinFET	
	A_{V_T}	A_{β_0}	A_{V_T}	A_{β_0}
	[mVμm]	[%μm]	[mVμm]	[%μm]
$w_{fin} = 10$ nm	2.7	1.5	2.4	1.1
$w_{fin} = 20$ nm	2.2	1.3	2.3	1.2

Interestingly all effects mentioned above are process related and can be minimized by process optimization in contrast to the dopant fluctuation induced mismatch which is given by statistics. Some of the effects mentioned above depend on transistor layout. Consequently matching optimized layout is required as shown in Chap. 4.

Matching is characterized on identical pairs of n- and p-type FinFETs featuring small fin widths down to 10 nm [54, 72]. To obtain the matching constants, the variances of threshold voltage V_T and current factor β are plotted against device area in the so called Pelgrom plot [42], see Fig. 2.10. The corresponding matching factors for n- and p-type FinFETs are summarized in Table 2.2. Very promising matching behavior is obtained even for narrow fins. Due to the optimization of fin patterning by means of etch process, annealing and OPC no serious degradation of matching behavior at small fins widths is observed as had been reported earlier in [71].

In conjunction with the high intrinsic gain particularly the promising matching behavior is a strong argument for the usage of fully depleted FinFETs in sub 32 nm CMOS technologies. In Chap. 4 a circuit example quantifies the potential performance and/or area benefits enabled by superior matching performance.

2.5 Charge-Trapping

Transient fluctuations of the threshold voltage in the mV regime induced by pro-
nounced charge-trapping is a new phenomenon in emerging CMOS technologies
comprising high-k dielectrics, independent of the device structure. To assess the im-
pact of this effect on analog and mixed-signal circuits charge trapping is character-
ized in detail regarding time constants, stress voltage and temperature dependence.
Based on the measurements an equivalent circuit model is derived to enable analog
circuit simulation. The measured devices feature high-k/metal gate stack similar to
the process published in [54]. The V_T shift is characterized by fast pulsed measure-
ments [73]. After initial V_T measurement the device under test is "stressed" with a
gate voltage pulse varying in pulse height and length. To determine amount and re-
covery of the V_T shift the threshold voltage is measured after the pulse with variable
delay.

   The approach to model transient V_T shifts derived in this work is shown in
Fig. 2.11. The ideas presented in [48] and [50] are extended to cover asymmetric
trapping and de-trapping time constants. The V_T shift is represented by a voltage
controlled voltage source V_{shift} in series with the gate. The controlling voltage itself
is derived by an equivalent sub-circuit model: a voltage controlled voltage source
V_{ss} applies the steady state V_T shift to an RC network. Steady state is defined as the
V_T shift which is measured at sufficient large (>1 ms) pulse width where no more
dependence on pulse width is observed, i.e. all traps are filled. The RC network mod-
els the distributed time constants resulting from the distributed traps, comparable to
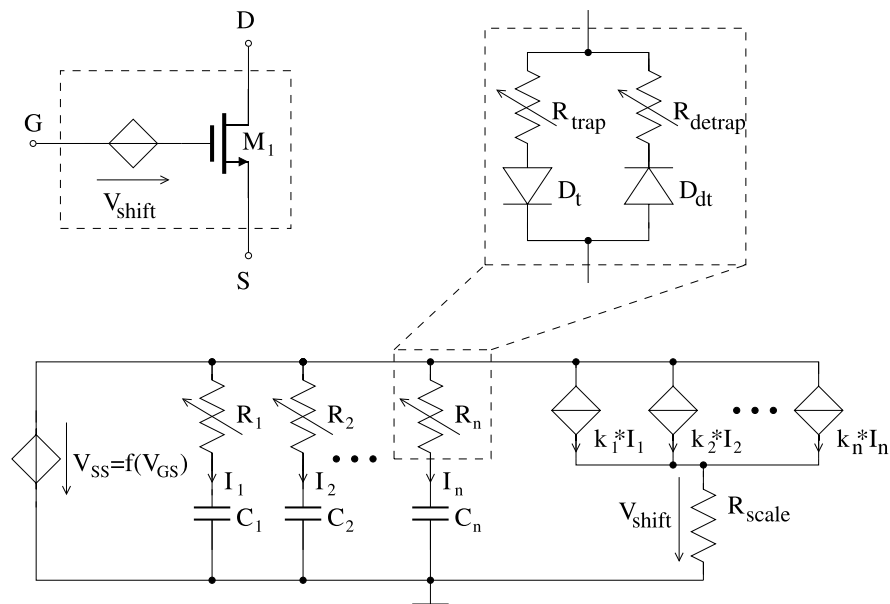
Fig. 2.11 Modeling of V_T shift as voltage controlled voltage source and implementation details
of the equivalent circuit for the control voltage
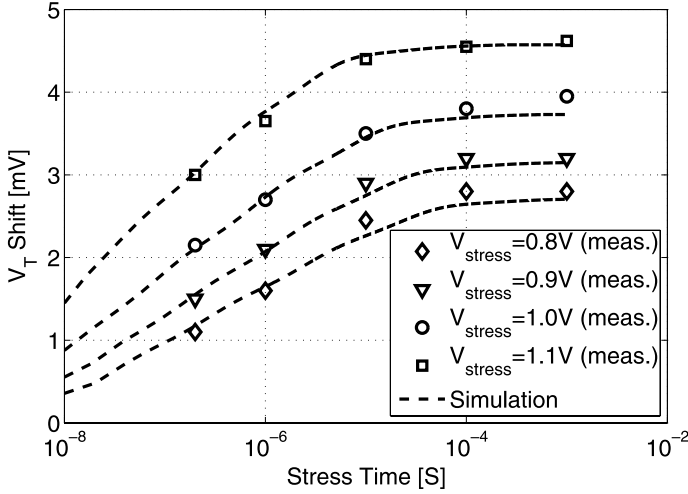
Fig. 2.12 Measured and simulated V_T shift for varying gate pulse height and length

simple flicker noise models. In contrast to [48] the resistors are voltage controlled to represent voltage dependent filling of traps. Different resistors are used for charging (trapping) and discharging (de-trapping). This approach allows to model asymmetric time constants for field enhanced trapping (positive gate pulse) and de-trapping (zero gate pulse or negative gate pulse). The RC current contributions $I_1, \ldots, I_n$ are weighted with scaling factors k_i in controlled current sources. The sum of the weighted currents induces a voltage drop over a the resistor R_{scale} which yields the final shift voltage. R_{scale} is a variable model parameter which can be used to set up different hysteresis scenarios.

To enable circuit simulation a set of model parameters is extracted from measurements. The V_{GS} dependence of the steady state V_T shift is modeled by means of a 4th order polynomial source V_{ss}. To reflect the hysteresis timing behavior properly 6 weighted[2] RC elements are used, covering trapping time constants from 10^{-8} s to 10^{-3} s and de-trapping time constants from 10^{-6} s to 10^{-1} s, respectively.

Measurement and simulation results are shown in Fig. 2.12 for varying gate pulse height and length. Three main statements are derived from these results: very fast traps with time constants below the μs regime have to be considered. Hence, the time constants of the effect are in a relevant range for typical analog and mixed-signal applications. Furthermore a strong dependence on the pulse height is observed, as shown in Fig. 2.13. As a consequence the mismatch of devices with different operation history will be significant. Finally the model enables a prediction of hysteresis behavior in circuit simulation with sufficient accuracy. The recovery behavior of the V_T shift is depicted in Fig. 2.14. As expected the de-trapping under zero gate bias occurs at much higher time constants than the field enhanced trapping. The differ-

---

[2]$k_1 = 1$, $k_2 = 1$, $k_3 = 1$, $k_4 = 0.84$, $k_5 = 0.15$, $k_6 = 0.05$.
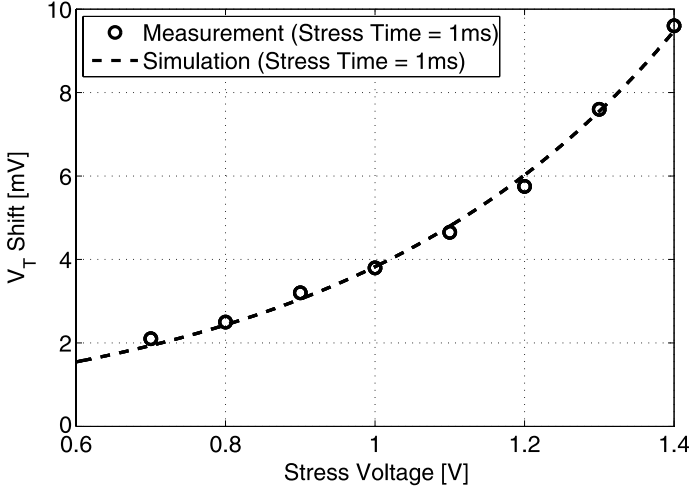
Fig. 2.13 Measured and simulated steady state V_T shift for varying gate pulse height
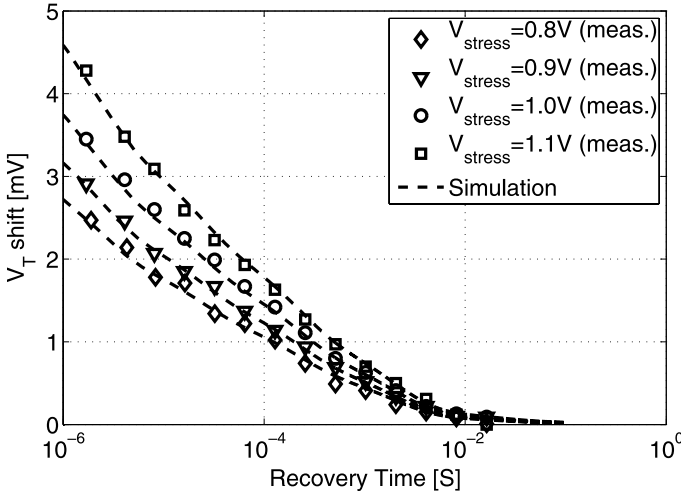
Fig. 2.14 Measured and simulated recovery of V_T shift for varying gate pulse height and measurement delay

ence amounts to about three orders of magnitude. It is noteworthy that negative gate pulses can accelerate de-trapping.

Measurement results reveal minor temperature dependence, no significant thermal activation of traps is observed. Therefore temperature effects are neglected in the circuit model. Overall, measurements and simulations are in close agreement. The model derived here serves as basis for the assessment on circuit level, using the scalability of the maximum V_T shift to simulate different hysteresis scenarios. Al-

though the absolute values of V_T hysteresis ($\approx$5 mV at 1 V stress) are representative for state-of-the-art high-k dielectrics, further process optimization may yield even lower levels [74]. Nevertheless the impact of V_T hysteresis on analog and mixed-signal circuits is studied in detail in this work. The motivation is twofold: one main goal of the investigation is to derive specifications for maximum tolerable V_T shift from analog perspective intended as feedback for technology development. On the other hand an early assessment of the impact on circuit level and development of corresponding countermeasures is required with regard to further scaling of CMOS technologies comprising novel material systems with possibly even higher V_T instabilities.

2.6 Self-Heating

The power dissipation in transistors leads to a local temperature increase, called self heating. Temperature changes affect transistor parameters such as carrier mobility or threshold voltage. At high gate-source and drain-source bias, i.e. at high current densities the reduction of the mobility is the dominant effect, resulting in a reduction of the drain current. As mentioned earlier the effect is particularly severe in SOI technologies due to the low thermal conductivity of the surrounding oxide (mainly the buried oxide layer) that acts as thermal insulator.

The impact of self heating on the output characteristics of an n-type FinFET is illustrated in Fig. 2.15(a). Pulsed measurements at different temperatures are compared to static measurement at room temperature. The pulse width is chosen very small in order to prevent self heating in these measurements. The DC measurement in contrast suffers from self heating and represents a kind of mean value of the pulsed measurements: at low V_{DS} values, i.e. at low power density it follows the room temperature curve, whereas at high V_{DS} values i.e. at high power density it converges to the 75°C curve. The maximum DC current is reduced by nearly 10%,
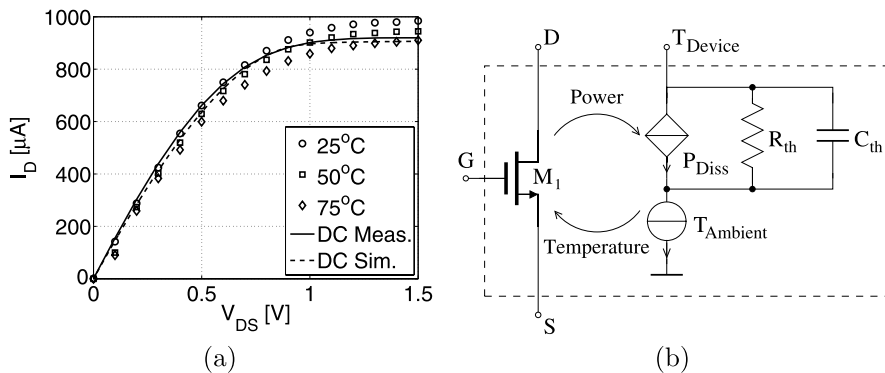

Fig. 2.15 Comparison of pulsed and DC I_D–V_{DS} measurements/simulation (**a**) and equivalent circuit model for self heating (**b**)

equivalent to a temperature rise of about 50°C. However, the power density in this example is larger than in typical analog use cases.

For analog circuit simulation self heating is modeled by means of electro-thermal coupling in a simplified equivalent circuit [75], as shown for a n-type FinFET in Fig. 2.15(b). The dissipated transistor power is sensed and applied via a controlled source to a thermal RC network comprising a thermal resistance R_{th} and a thermal capacitance C_{th}. R_{th} is defined as temperature increase per dissipated power: $R_{th} = \Delta T / P$. C_{th} is used to fit the time dependence. The model can be easily extended to cover multiple time constants [76]. The thermal parameters R_{th} and C_{th} are extracted by pulsed measurements, RF small signal measurements [77] or device simulations [76]. For typical FinFET device dimensions R_{th} is in the range of 10°K/mW to 100°K/mW, the respective time constants are in the 10–100 ns regime [50, 76]. Figure 2.15(a) shows that the simulations fit well the measured data.

Similar to charge trapping self-heating yields history dependent transistor behavior and potential dynamic mismatch effects. The impact on analog and mixed-signal circuits is discussed in Chap. 4. Since self-heating is strongly affected by the device geometry the scaling behavior of self-heating is analyzed next. To avoid the need for complex and time consuming device simulations a simplified approach is used [78]. The complex 3D FinFET structure is partitioned in individual basic blocks in such a way that the thermal resistance of the basic blocks can be analytically calculated. The model includes gate stack, source and drain landing pads, source, drain and gate contacts as main heat conductors and is calibrated with device simulations and measurements. In this way the impact of geometry variations can be easily assessed.

The fin width is a key scaling parameter for FinFETs due to its impact on electrostatic integrity. The dependence of the thermal resistance on the fin width for constant gate length of 45 nm and 8 fins in parallel is shown in Fig. 2.16(a). As expected, with decreasing fin width, i.e. with decreasing silicon volume the thermal resistance increases up to a factor of two. However, in a realistic scaling scenario not only the fin width but almost all dimensions are reduced. In Fig. 2.16(b) the thermal

(a)   (b)
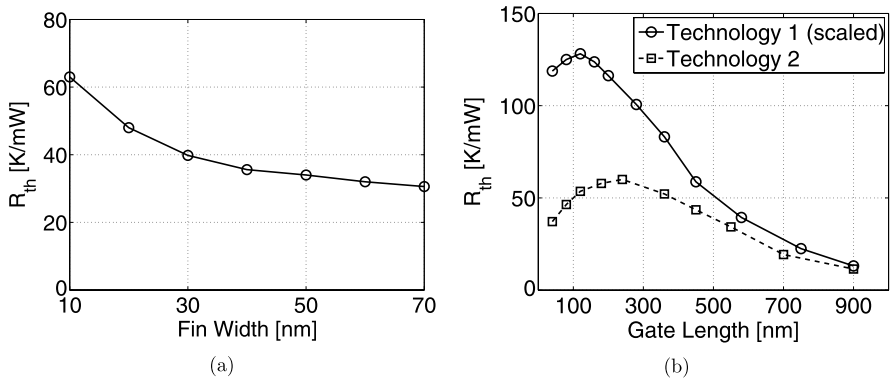
Fig. 2.16 Simulated scaling behavior of thermal resistance with regard to fin width (**a**) and all relevant dimensions (**b**)

resistance of two FinFET technologies is compared. Technology 2 refers to typical dimensions as used in [6]. Technology 1 represents a down-scaled technology, assuming a scaling factor of 0.7 applied to minimum gate length, fin width, fin pitch, contact and metal dimensions, contact density and thickness of buried oxide layer. The thermal resistance increases up to a factor of 2 in this example. The conclusion drawn from these simulations is that the impact of self-heating on device behavior is increasing with technology scaling and has to be considered in design and layout.

Springer