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Advanced Gate Stacks for High-Mobility Semiconductors

Bearbeitet von
Athanasios Dimoulas, Evgeni Gusev, Paul C McIntyre, Marc Heyns

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Strained-Si CMOS Technology

S. Takagi

Summary. Improvement in performance of Si MOSFETs through conventional device scaling has become more difficult, because of several physical limitations associated with the device miniaturization. Thus, much attention has recently been paid to the mobility enhancement technology through applying strain into CMOS channels. This chapter reviews this strained-Si CMOS technology with an emphasis on the mechanism of mobility enhancement due to strain. The device physics for improving drive current of MOSFETs is summarized from the viewpoint of electronic states of carriers in inversion layers and, in particular, the subband structures. In addition, recent experimental results on implementing strain into CMOS channels are described.

1.1 Introduction

A guiding principle of performance enhancement in Si CMOS has been the scaling law over 30 years. Under 90 nm technology node and beyond, however, the performance enhancement of CMOS through the device scaling such as shrinking the gate length and thinning the gate oxide has become more and more difficult, because of several physical limitations in miniaturization of MOSFETs. For example, thinning the gate oxide, needed to reduce the supply voltage, leads to the rapid increase in gate tunnelling current. Also, the increase in substrate impurity concentration, needed to suppress short channel effects, leads to the reduction in carrier mobility and resulting decrease in the on-current [1]. As a result, simple device scaling encounters a trade-off relationship among the current drive, the power consumption and the short-channel effects, all of which are quite important factors for LSI applications.

Thus, the device technologies using new channel structures and new channel materials, which mitigate the stringent constrains regarding the device design, have recently stirred a strong interest, in addition to high-k gate insulator technologies. These device technologies, called "Technology Boosters" in ITRS 2004 edition [2], include strained Si channels, ultrathin SOI, metal gate electrodes, multigate structures, ballistic transport channels, metal source/drain

junctions, and so on. Among them, strained-Si channels [3–6] have been recognized as a technology applicable to near term technology nodes, thanks to the recent progress in so-called "local strain techniques", and have actually been included in 90 nm logic CMOS technologies [7]. The mobility enhancement obtained by applying appropriate strain, can provide higher carrier velocity in MOS channels, resulting in higher current drive under fixed supply voltage and gate oxide thickness. This means that thicker gate oxides and/or lower supply voltage can be used under a fixed current drive, leading to the mitigation of the trade-off relationship among current drive, power consumption and short-channel effects. As a result, the strain engineering and resulting increase in channel mobility has been regarded as a device technology mandatory in future technology nodes, as well.

This chapter reviews the principle and the device application of this strained-Si CMOS technology with an emphasis on the physical mechanism of mobility enhancement due to strain.

1.2 Impact of Mobility Enhancement on Current Drive of Short-Channel MOSFETs

In short channel MOSFETs, the modelling of the current drive is not straightforward, because of the co-existence of the velocity saturation effect due to high lateral electric field and the non-stationary transport effect, caused by the fact that carriers in ultra-short channels travel from source to drain without encountering sufficient scattering events. Furthermore, it is expected that ballistic transport [8], where carriers have no scattering in channels, can be realized in extremely-short channels less than 10 nm. Thus, quasi-ballistic transport models [9,10] to describe the current drive by considering a small number of scattering events have been proposed on a basis of full ballistic motion.

Figure 1.1(a, b) shows the schematic diagrams of factors that dominate current drive under a classical drift model and a quasi-ballistic model, respectively. In both models, the drive current is described by the product of surface carrier concentration and velocity near the source region. Since the surface carrier concentration is constant under fixed values of gate insulator thickness, threshold voltage and gate voltage, the increase in the carrier velocity near source region is needed for the enhancement of the drive current.

In the drift model, the velocity near source region is strongly affected under non-stationary transport by low-field mobility near source region, while the velocity near source region in the quasi-ballistic model is determined by the injection velocity from source and the back-scattering rate into source [9, 10], which are also given by low-field mobility near source region. As a consequence, the increase in low-field mobility near source region can lead to the enhancement of the drive current in short channel devices, in both models.

Actually, it has been reported from the simulation results of carrier velocity and drive current in strained-Si n-MOSFETs with gate length of 100 nm that

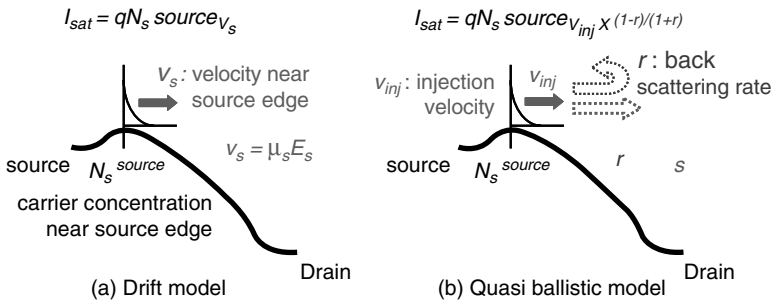

Fig. 1.1. Schematic diagrams to show factors to dominate current drive, I_{sat}. Fig. 1.1(**a**) and (**b**) show the diagrams based on a classical drift model and a quasi-ballistic model, respectively. E_s, q and μ_s mean the lateral electric field, the elementary charge and mobility near source region, respectively

the increase in mobility can provide the increased velocity and resulting higher drive current under a constant saturation velocity model [11]. Also, recent experimental and theoretical results [9,12,13] have shown that the drive current of MOSFETs with gate lengths of 100–50 nm is roughly proportional to the square root of low-field mobility. These results strongly suggest that low-field mobility is still important for the current drive in short-channel MOSFETs.

On the other hand, carrier velocity is also affected by the scattering probability of high energy carriers, typically reflecting in the energy relaxation time. As described below, strain induces band splitting, which can lead to longer energy relaxation time and resulting higher velocity [11]. Thus, device simulations accurately taking non-stationary transport effects and detailed band structures into account are mandatory for quantitative understanding of the current drive of short-channel MOSFETs.

1.3 Physical Mechanism of Mobility Enhancement in Strained-Si n- and p-Channel MOSFETs

1.3.1 Physical Origin of Mobility Enhancement in n-Channel MOSFETs

Before explaining the physical origin of mobility enhancement due to strain, it is necessary to describe the electronic properties of Si MOS inversion layers. Figure 1.2 schematically shows the equi-energy surfaces of inversion-layer electrons in the two-dimensional subband structure on a (100) surface and the characteristics of the valley structures. The conduction band in bulk Si is composed of six equivalent valleys. In inversion layers, on the other hand, these six valleys are split into the twofold valleys locating at a central position in two-dimensional k-space and the fourfold valleys locating on k_x and k_y axes, because of two-dimensional quantization. Three-dimensional

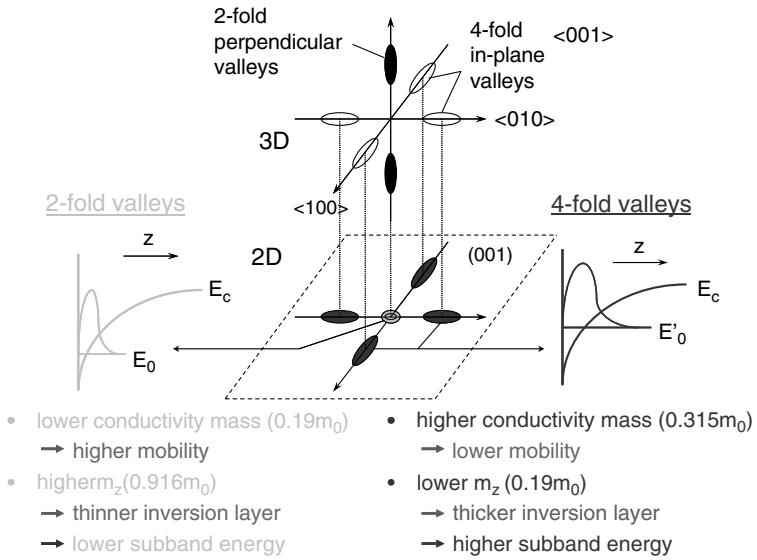

Fig. 1.2. Schematic diagram of characteristics of the two- and four-fold valleys in two-dimensional electrons on a (100) surface

electrons have an anisotropy in the effective mass, composed of light transversal effective mass, $m_{\rm t}(= 0.19\,m_0)$, where m_0 is the electron mass in free space, and the heavy longitudinal effective mass, $m_{\rm l}(= 0.916\,m_0)$. As a result, the twofold degenerate valleys have the effective masses of $m_{\rm t}$ in parallel and $m_{\rm l}$ in perpendicular to MOS interfaces, while the fourfold degenerate valleys have the effective masses of $m_{\rm t}$ and $m_{\rm l}$ in parallel and $m_{\rm t}$ in perpendicular to MOS interfaces.

This difference in the effective mass leads to a variety of differences in physical properties between the twofold and the fourfold valleys. For instance, the conductivity mass parallel to MOS interfaces is lower in the twofold valleys than in the fourfold valleys and, thus, the mobility of electrons in the twofold valleys becomes higher than that in the fourfold valleys. Also, since the thickness of inversion layers and the subband energy are determined by the effective mass perpendicular to MOS interfaces, the thickness of the inversion layers is thinner and the subband energy is lower in the twofold valleys having higher effective mass perpendicular to the MOS interfaces than in the fourfold valleys.

The impact of strain on the electron mobility in n-channel Si MOSFETS can also be understood in terms of this subband structure or valley structure [14]. Figure 1.3 schematically shows the effect of tensile strain on the subband structures. The electron occupancy of the twofold and the fourfold valleys at room temperature is almost the same without any strain. This is because the lower subband energy of the twofold valleys is compensated by the higher density-of-states of the fourfold valleys having the higher valley

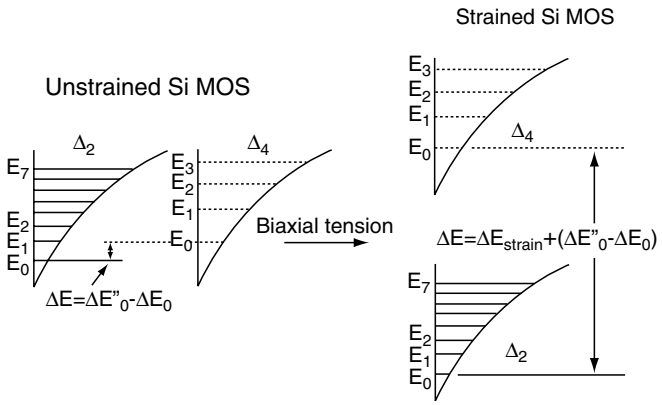

Fig. 1.3. Energy lineups of the Si conduction band in the inversion layer with and without tensile strain

degeneracy and the higher density-of-state mass. When tensile strain parallel to MOS interfaces or compressive strain perpendicular to MOS interfaces is applied to MOSFETs, the conduction band edge in the fourfold valleys becomes higher than that in the twofold valleys and this splitting energy is added to the subband energy difference caused by the surface quantization. As a result, the subband energy between the two valleys significantly increases.

This increase in the subband energy splitting yields an increase in the inversion-layer mobility through the following two mechanisms. One is the increase in the averaged mobility due to the increase in the occupancy of electrons in the twofold valleys having higher mobility. The other is the suppression of inter-valley scattering between the twofold and the fourfold valleys. This is because, when the splitting energy between the twofold and the fourfold valleys is higher than the phonon energies associated with inter-valley scattering, the transition of electrons in the twofold valleys through a phonon absorption process cannot occur, resulting in the reduction in the scattering probability. Since the inter-valley scattering has a large contribution to the total scattering rate of Si MOSFETs at room temperature and the influence becomes larger with an increase in temperature, this increase in the mobility due to tensile strain is more effective in enhancing LSI performance during real operation at temperatures higher than room temperature.

On the other hand, when compressive strain parallel to MOS interfaces or tensile strain perpendicular to MOS interfaces is applied to MOSFETs, the electron mobility tends to decrease. This is attributable to the increase in the occupancy of the electrons in the fourfold valleys having lower mobility.

The change in the conductivity in Si by applying mechanical strain is well known as the piezo-resistance effect and the experimental data for bulk Si has been reported 50 years ago [15]. The experimental results of the piezo-resistance effect on Si MOSFETs have also been reported extensively [16–18]. Here, the characteristics of mechanical strain are, in general, that the amount

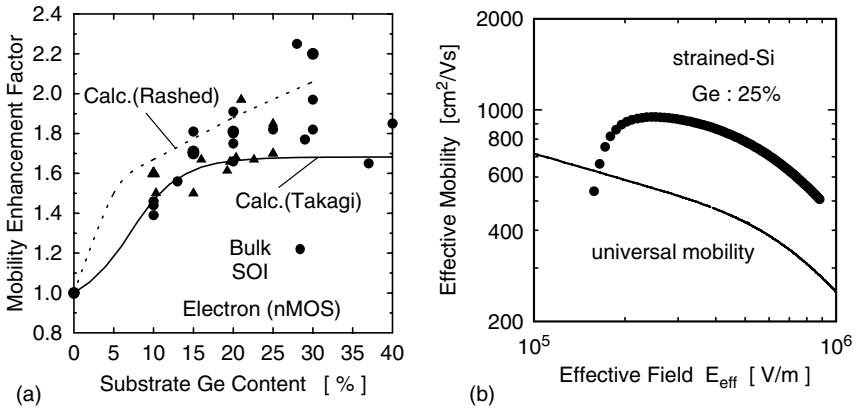

Fig. 1.4. Mobility characteristics of bi-axial strained-Si n-channel MOSFETs (**a**) Mobility enhancement factor as a function of Ge content in SiGe substrates, which is in proportion to strain. Strained Si on relaxed SiGe with Ge content of 24 at % has strain of 1%. *Closed circles* and *triangles* show the experimental values in bulk and SOI MOSFETs, respectively. *Solid* [14] and *dash* [32] *lines* mean the results of theoretical calculations. (**b**) Effective field ($E_{\rm eff}$) dependence of electron mobility in bi-axial strained-Si nMOSFETs

of the strain is small and the strain configuration is uni-axial. It has been shown for n-channel MOSFETs that mechanical tensile strain leads to a mobility increase [17, 18], also attributed to the subband energy splitting. As a consequence, since a primary parameter for the mobility enhancement in n-channel MOSFETs is the subband energy splitting between the twofold and the fourfold valleys, there exists no essential difference in physical mechanism for mobility modulation due to bi-axial and uni-axial strain, though a quantitative difference in the amount of the enhancement is seen.

The relationship between electron mobility in n-channel MOSFETs and bi-axis tensile strain parallel to MOS interfaces has been systematically investigated by using strained-Si MOSFETs fabricated on relaxed SiGe substrates. Figure 1.4(a) shows the experimental results for the mobility enhancement factor [19–31], defined by the ratio of the mobility in strained-Si MOSFETs to that in conventional (unstrained) Si MOSFETs, as a function of Ge content in SiGe substrates. Here, strain in Si on relaxed SiGe with Ge content of 24 at % amounts to strain of 1%. Results of the enhancement factor theoretically calculated on the basis of phonon scattering are also shown [14, 32]. Agreement between the experimental and theoretical results is fairly good. It is found that maximum an enhancement factor of roughly two is obtained.

Figure 1.4(b) shows the effective field ($E_{\rm eff}$) dependence of electron mobility in n-channel MOSFETs at room temperature with and without tensile strain [29, 33]. It is found that the mobility enhancement factor is almost constant, irrespective of $E_{\rm eff}$. Since the mobility in moderate $E_{\rm eff}$ region is known to be dominated by phonon scattering, the mobility enhancement in this

region can be explained by the mechanisms described above. In high E_{eff} region, on the other hand, almost all the electrons can occupy the twofold valleys even without any strain, because of the increased confinement caused by strong surface electric field. Since this fact suggests that the band splitting might have much less influence on the mobility in high E_{eff} region, the high enhancement factor experimentally observed in high E_{eff} region has been attributed to the reduction in the probability of surface roughness scattering [34], which dominates the mobility in high E_{eff} region. However, the physical origin is still unclear because of the lack of direct evidence for the decreased surface roughness scattering.

1.3.2 Physical Origin of Mobility Enhancement in p-Channel MOSFETs

Compared with n-channel MOSFETs, the impact of strain on hole mobility in p-channel MOSFETs is complicated and the physical mechanism has not been fully and quantitatively understood yet. Also, it has recently been recognized in p-channel MOSFETs that the effects of uni-axial and bi-axial strain on the hole mobility are significantly different [7, 35–37], which is in contrast to n-channel MOSFETs. It has been pointed out that uni-axial compressive strain perpendicular to channel direction and bi-axial tensile strain are effective in enhancing the hole mobility in p-channel MOSFETs [38].

Figure 1.5 shows the results of theoretical calculations of the three-dimensional Si valence band structure near the Γ point with uni-axial compressive strain and bi-axial tensile strain [38]. Here, assuming a MOSFET channel direction as parallel to ⟨110⟩, the strain directions are taken to be parallel to (001) surface for bi-axial strain and in the ⟨110⟩ direction for uni-axial strain. The right and the left directions of are horizontal axes in the figures in the wave vectors perpendicular to the MOS interface (along ⟨001⟩ direction) and parallel to the channel (along ⟨110⟩ direction), respectively. While, without any strain, the heavy hole band and the light hole band degenerate at the top of the valence band, the application of strain leads to the band splitting and shifting the light hole band upward. As a result, the top of the valence band is composed of the light hole band. In addition, the modulation of the curvature of the bands due to strain provides a change in the effective mass and the anisotropy in the effective mass parallel and perpendicular to the MOS interface. As a consequence, hole mobility enhancement due to strain is attributable to the following three mechanisms: (1) reduction in the effective mass of occupied bands; (2) suppression of inter-subband scattering due to the subband energy splitting; (3) increase in the occupancy of subbands having higher mobility.

Figure 1.6(a) shows experimental results of the hole mobility enhancement factor in bi-axial tensile-strained Si p-MOSFETs fabricated on relaxed SiGe substrates as a function of Ge content in the SiGe substrates [20, 22, 26, 28–30, 39–45]. The theoretically calculated results of the enhancement factor are

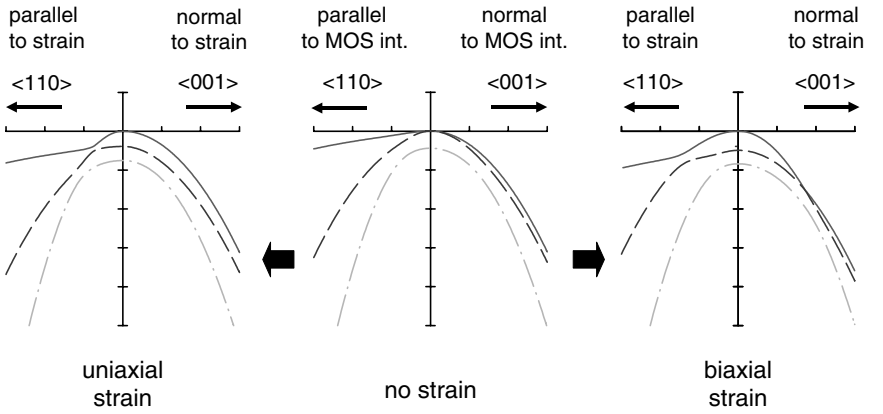

Fig. 1.5. Results of theoretical calculations of the change in the Si valence band structure near the Γ point with uni-axial compressive strain and bi-axial tensile strain [38]. The strain directions of the uni-axial and the bi-axial strain are parallel to ⟨110⟩ direction and (001) surface, respectively. The channel direction is assumed parallel to ⟨110⟩ direction. The right and the left directions of the horizontal axes correspond to wave vectors perpendicular to the MOS interface (⟨001⟩ direction) and parallel to the channel (⟨110⟩ direction), respectively. Without any strain (the center figure), *solid*, *dash* and *dotted dash lines* correspond to heavy hole band, light hole band and split-off band, respectively

also shown [46, 47]. It is found that, with a Ge content of 30% or higher, an enhancement factor of roughly two can be obtained, while the enhancement factor is small with low Ge content. Figure 1.6(b) shows the experimental $E_{\rm eff}$ dependence of hole mobility in bi-axial tensile strain Si p-MOSFETs at room temperature. It is found [29,44] that the hole mobility enhancement factor decreases with an increase in $E_{\rm eff}$. Note here that the values of the enhancement factor plotted in Fig. 1.6(a) are the maximum ones in the lower $E_{\rm eff}$ region. Since the mobility at high $E_{\rm eff}$ is important for practical applications it is necessary to use tensile-strained Si films with high Ge content and a resulting high strain for bi-axial tensile strained Si p-MOSFETs.

It has recently been recognized [7, 35–37] that, when uni-axial compressive strain is applied along ⟨110⟩ direction to p-MOS channels parallel to ⟨110⟩, the hole mobility enhancement is higher for rather small strain magnitude and is not significantly reduced by increasing $E_{\rm eff}$. Figure 1.7 shows the experimental $E_{\rm eff}$ dependence of hole mobility in Si p-channel MOSFETs with uni-axial compressive and bi-axial tensile strain [36]. It is confirmed that a higher enhancement factor in the high $E_{\rm eff}$ region can be maintained for uni-axial strain.

It has been, on the other hand, reported [16, 18] in measurements of the piezo-resistance of (100) surface Si p-channel MOSFETs by using uni-axial mechanical strain that compressive strain parallel to the channel direction and tensile strain parallel to channel width increase the hole mobility. These

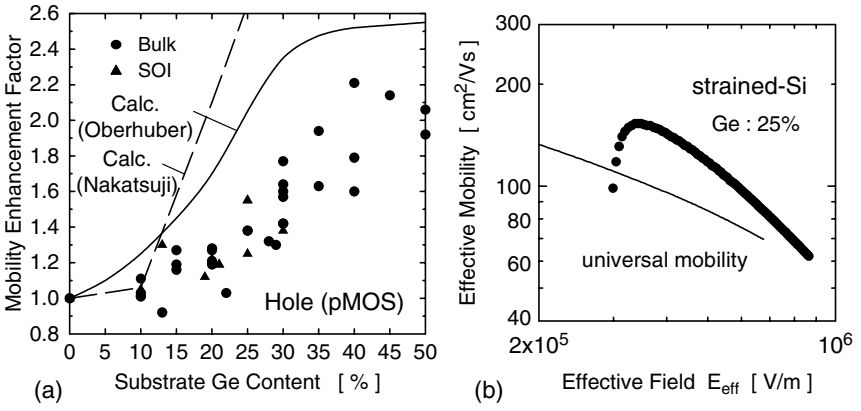

Fig. 1.6. Mobility characteristics of bi-axial tensile strained Si p-channel MOSFETs (**a**) Mobility enhancement factor as a function of Ge content in SiGe substrates. *Symbols* show experimental results. *Closed circles* and *triangles* show the values in bulk and SOI MOSFETs, respectively. *Solid* [46] and *dash* [47] *lines* mean the results of theoretical calculations. (**b**) $E_{\rm eff}$ dependence of hole mobility in bi-axial tensile-strain Si p-channel MOSFETs

complicated dependencies of strain on hole mobility in p-channel MOSFETs can be roughly summarized by Fig. 1.8, which have been obtained by the recent theoretical calculations [38]. For small strain magnitude, typically seen in piezo-resistance measurements by applying mechanical strain, compressive strain parallel to ⟨110⟩ channel direction (tensile strain parallel to channel width) increases the hole mobility. On the other hand, when the amount of

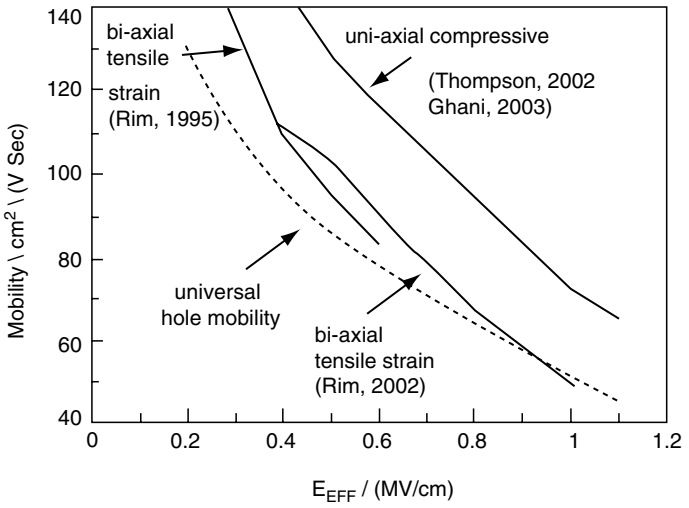

Fig. 1.7. Experimental results of the $E_{\rm eff}$ dependence of hole mobility in Si p-channel MOSFETs with uni-axial compressive and bi-axial tensile strain

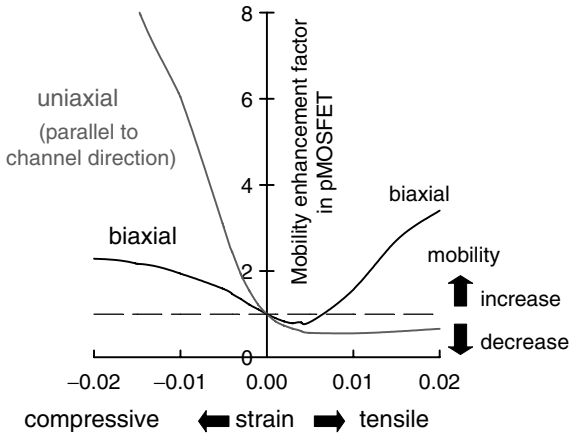

Fig. 1.8. Calculated results of the mobility enhancement factor for inversion-layer holes in Si p-channel MOSFETs with uni-axial compressive and bi-axial tensile strain [38]. The value of $E_{\rm eff}$ is taken to be $1\,{\rm MV\,cm^{-1}}$

strain increases to some extent, both compressive and tensile bi-axial strain also increase the hole mobility and, in particular, the mobility enhancement by tensile bi-axial strain becomes higher. It can be understood from these results that uni-axial compressive strain parallel to $\langle 110 \rangle$ channels is most effective for the hole mobility enhancement in p-channel MOSFETs and, if the amount of strain is large, bi-axial tensile strain are effective.

The difference in the $E_{\rm eff}$ dependence of the hole mobility in Si p-channel MOSFETs between uni-axial compressive and bi-axial tensile strain has been explained by the difference in the physical mechanism for hole mobility enhancement for the two strain configurations. The hole mobility enhancement for bi-axial tensile strain has been attributed mainly to the suppression of inter-band scattering due to the band splitting between heavy hole and light hole bands and less to the contribution of the change in the effective mass due to strain [36, 37]. In addition, the effective mass perpendicular to MOS interfaces in the subband originating in the light hole band, which is lower in energy, is lighter than that in the subband originating in the heavy hole band, as seen in the right figure of Fig. 1.5. As a result, the increase in the subband energy due to carrier confinement at MOS interfaces is higher in the light hole band than in the heavy hole band. Since this increase in the subband energy due to confinement reduces the strain-induced energy difference between the light hole and heavy hole bands, the total amount of band splitting reduces with an increase in $E_{\rm eff}$ and, finally, the heavy hole band becomes higher in energy than the light hole one. This change in the band splitting has been regarded as a main cause for the decrease in the mobility enhancement in bi-axial tensile strain p-MOSFETs with increasing $E_{\rm eff}$. [36–38, 48–50]

In contrast, the hole mobility enhancement by uni-axial compressive strain has been attributed both to a decrease in the effective mass associated with

the strain and to the suppression of inter-band scattering [36–38, 51]. In addition, contrary to bi-axial tensile strain, the effective mass perpendicular to MOS interfaces in the subband originating in the light hole band is heavier than that in the heavy hole band, as seen in the left figure of Fig. 1.5. Therefore, the increase in the subband energy difference between the light hole and the heavy hole subband due to carrier confinement is added to the strain-induced energy difference, leading to a further increase in the subband energy difference and a resulting increase in the occupancy of the lowest subband having the lower effective mass. Since this effect becomes more evident with increasing E_{eff}, higher hole mobility enhancement is maintained for uni-axial compressive strain. As a result, the difference in the E_{eff} dependence of hole mobility between uni-axial compressive and bi-axial tensile strain has been ascribed to the difference in the influence of the uni-axial and the bi-axial strain on the band structure, particularly, to the difference in the effective mass perpendicular to MOS interfaces.

While these interpretations are based on the recent band calculations, they have not been fully established yet, because of the complicated valence band structure in Si and the differences in the interpretations [47, 51] existing among the various calculation models. Further investigations of the transport properties of inversion-layer holes in strained-Si MOSFETs are clearly needed, from both the theoretical and experimental viewpoints.

1.4 Implementation of Strain into MOSFETs

1.4.1 Global Strain Technology

As a device structure with a bi-axial tensile strained channel, MOSFETs on strained-Si layers epitaxially grown on relaxed SiGe substrates, which have a larger lattice constant than Si, have been extensively studied [3–6,52]. Furthermore, a variety of new substrates and device structures such as strained-Si-On-Insulator (Strained-SOI) MOSFETs [6, 53, 54], where strained-Si/relaxed SiGe layers are formed on buried oxides, and Strained-Si-directly-On-Insulator (SSDOI) MOSFETs [55, 56], where straind-Si layers are directly bonded to buried oxides, have been proposed and demonstrated as modified versions of bulk strained-Si MOSFETs. Typical substrates and device structures using these bi-axial tensile strained films are schematically shown in Fig. 1.9. The technologies to fabricate MOSFETs on wafers over which strained-Si layers are formed have recently been called "*Global strain technology*".

As for MOSFETs using these global strain Si substrates, the research and development on device optimization have currently been conducted for applications to 45 nm technology and beyond. Figure 1.10 shows a TEM photograph of one example of strained-SOI MOSFETs with gate length of 32 nm [31]. Many research groups have already reported improvement in on-current of around 10–25% with global strain Si MOSFETs, with short gate lengths less

(*I*) *Global strain technology*

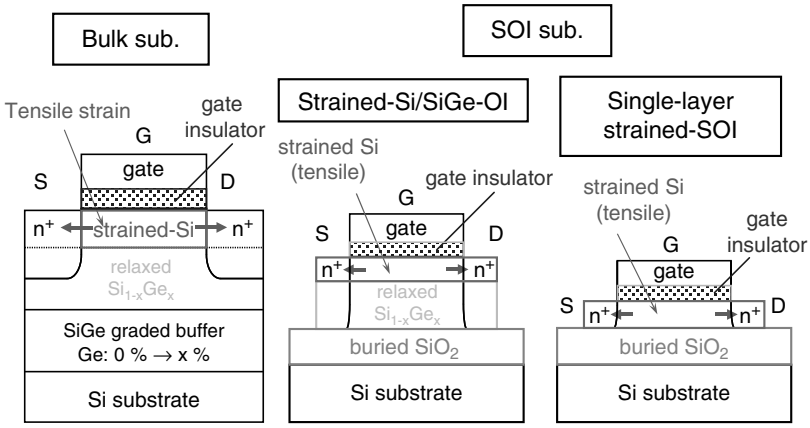

Fig. 1.9. Schematic cross-sections of typical MOS structures using global bi-axial tensile strain

than sub-100 nm [31, 56–63]. The successful operation of CMOS with gate length of 25 nm [58] and the integration of strained-Si MOSFETs with high-k gate insulators [64] and metal gates [59] have also been demonstrated.

Advantages of global strain Si MOSFETs are listed as follows: (1) large and uniform strain can be realized; (2) conventional CMOS fabrication processes can be applied with minimal modification for global strain substrates supplied from wafer vendors. On the other hand, there are still many issues for practical

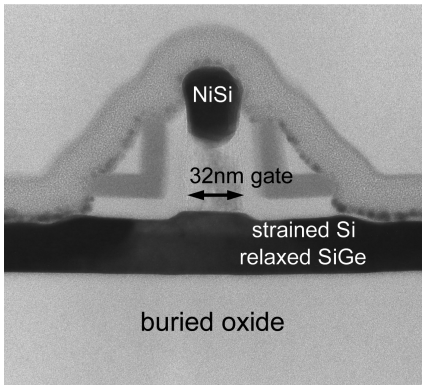

Fig. 1.10. TEM photograph of cross-sectional view of a strained Si-On-Insulator MOSFET with gate length of 32 nm [31]. A trained-Si thin film, where a channel of the MOSFET is formed, and a relaxed-SiGe thin film are fabricated on a buried oxide layer. The gate electrode is made of poly-Si and NiSi formed in source/drain region and on the top of the poly-Si gate

use of this technology. For example, (1) limited performance improvement in p-channel MOSFETs with small or moderate strain (2) wafer quality including defects and dislocations (3) wafer cost (4) increase in junction leakage current. Also, the importance of reducing the parasitic resistance in source/drain regions has been pointed out for higher performance enhancement in ultra-short gate lengths [31, 63].

1.4.2 Local Strain Technology

As a technology to solve the above issues associated with global strain techniques, "*local strain technology*", which introduces structures and materials to induce strain into channels locally inside MOSFETs, has recently stirred keen interest. Figure 1.11 schematically shows a variety of local strain technologies. In particular, the following two methods are quite typical.

(1) *SiGe source/drain*. SiGe is epitaxially grown selectively in source/drain regions, where are etched off toward substrates. These buried SiGe regions induce uni-axial compressive strain into channels, applied to p-channel MOSFETs [7, 35]. Recently, n-channel MOSFETs with tensile strain induced by selectively growing SiC in source/drain regions instead of SiGe have also been reported [65].
(2) *SiN capping layer*. SiN capping layers with intrinsic stress, deposited on MOSFETs as interlayer films, induce strain into MOS channels [66–68]. In many cases, SiN films with tensile strain have been applied to n-channel MOSFETs, while SiN films with compressive strain have recently been developed and used for p-channel MOSFETs [69].

Besides these approaches local strain from isolation regions like shallow trench isolation [70], poly-gate electrodes [71], silicide regions [72], etc. can also be used. Judging from the fact that /SiGe source/drain and strained SiN capping layers has been applied to logic LSI processes under 90 nm technology

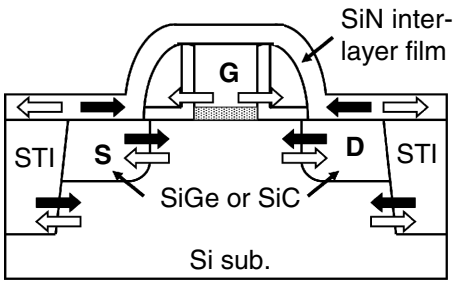

Fig. 1.11. Schematic illustration of a device structure using a variety of local strain techniques. STI in the figure means regions of Shallow Trench Isolation. *Black and white* arrows indicate compressive and tensile strain, respectively

node for mass production [7, 35], these local strain technologies have already become quite practical.

It should be noted that most of these techniques tend to produce high strain along a specific direction (uni-axial strain). Actually, the experimental results of uni-axial strain in Fig. 1.7 have been obtained from MOSFETs with SiGe source/drain, above described [7, 35–37]. Advantages of the local strain technologies are listed as follows: (1) since the standard CMOS processes can be used with minor changes and novel wafers are not needed, the implementation is easy and the production cost is low; (2) By using uni-axial strain, high performance enhancement of p-channel MOSFETs can be obtained even with comparatively small amount of strain.

Owing to these advantages, introduction and the optimization of local strain techniques are, at present, being conducted extensively for near term technology nodes. Furthermore, a variety of new structures and new techniques that enables one combine local strain technology with future CMOS structures remain under investigation.

As for local strain technology, on the other hand, issues to be solved are: (1) the amount of strain and the resulting performance boost could be limited; (2) since the strain profile in the channels is non-uniform and the amount of strain is strongly dependent on device geometries and dimensions, variation in electrical characteristics could be large; (3) the circuit design is not easy, because of the geometry dependence of strain.

In addition, an important concern in any strained Si CMOS technologies including the global and the local ones is strain relaxation, which may come from subsequent processing or from the device geometry. It is, in the simplest case, well known that the strain in strained films patterned into isolated areas is relaxed from their edges. Actually, uni-axial strain has been created on bi-axial global strain substrates by utilizing this phenomenon [73, 74]. However, any unintentional strain relaxations have to be avoided by carefully designing the process conditions and the device geometry, though the robustness against strain relaxation can be strongly dependent on the strain-application techniques. It should be noted here that local strain evaluation techniques that probe the strain distribution inside small devices with high spatial resolution are of paramount importance for this purpose.

1.5 Conclusions

The strained-Si CMOS technology has been regarded as mandatory for future technology nodes, because of the necessity to maintain high current drive. On the other hand, a future important goal for strained-Si technology is to establish methods of applying strain that are compatible with a variety of other technology boosters such as high k/metal gate technology and multi-gate structures. Thus, a future direction for research and the development includes the optimal design of strain profiles in future CMOS struc-

tures and their realization through global strain techniques, local strain techniques or their combination. Device/process designs for the robustness against performance variation and avoidance of reliability problems can are also other important priorities. In order to accomplish these tasks, further comprehensive and quantitative understanding of the effects of strain on electrical characteristics and fabrication processes as well as the metrology of strain with high resolution are strongly needed.

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