Chapter 2
Thin Chips on the ITRS Roadmap

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Abstract The International Technology Roadmap for Semiconductors (ITRS) projects decreasing chip thickness in support of three-dimensional integrated circuit (3D IC) solutions. The 3D IC technology potential is not yet fully leveraged due to insufficient scaling of the through-silicon via (TSV) pitch. Since technological limits restrict the TSV ratio at about 10:1, minimum chip thickness enables us to take full advantage of the 3D IC concept in support of continued miniaturisation (More Moore). Moreover, the excellent mechanical properties of silicon qualify ultra-thin chips for applications of silicon technology for added functionality (More than Moore).

2.1 The ITRS Roadmap

In 1965 Gordon E. Moore presented his vision about the future exponential growth of the semiconductor industry, known today as 'Moore's Law' [1]. Following Moore's prediction the industry has kept a steady pace of miniaturisation, doubling device density every 18–24 months, doing so for 45 years now. It was not only about forecasting, but about commanding the silicon revolution. The idea has evolved into a more specific definition, a roadmap that is defined by semiconductor manufacturers and equipment providers.

Since the 1992 publication of the National Technology Roadmap for Semiconductors in the United States by the Semiconductor Industry Association (SIA), with new versions in 1994, 1997, and 1999, this treatise has been widely quoted throughout the industry [2]. Since 1998 the International Roadmap for Semiconductors (ITRS) has represented an international effort toward improving semiconductor device scaling by combining various national or regional roadmap initiatives worldwide, such as the European Electronic Component Manufacturers'

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Association (EECA), the Electronic Industries Association of Japan (EIAJ), the Korea Semiconductor Industry Association (KSIA) and the Taiwan Semiconductor Industry Association (TSIA), besides SIA. Over the years ITRS has become the global industry's metronome, setting the pace for the development of new semiconductor technologies. Due to the fast-paced nature of the industry the roadmap needs to be reviewed annually. The international ITRS consortium with experts from over 900 companies organised in working groups projects the technological needs for the next 15 years on an annual basis.

2.2 Thin Chips for More Moore

The 2001 edition of the ITRS mentions for the first time about a need for thin dies to allow for three-dimensional (3D) chip stacking in system-in-package (SiP) solutions. In the 2003 edition very thin dies are mentioned, though not yet with a defined thickness target; only a forecast on the number of stacked dies was made. The 2005 ITRS edition put a strongly increased focus on wafer thinning and handling, small and thin die assembly and packaging of thin chips. A need for chips thinner than 20 μm was mentioned. Wafer thinning was the only technique considered for achieving thin chips. It was projected that at thicknesses below 10 μm a sequential combination of mechanical grinding, chemical–mechanical polishing (CMP), wet etching and plasma treatment, and dry chemical etching would be required to allow for control of such small chip thickness and to produce a die free of stress. The development of new pick and place techniques was viewed as a key issue for handling and assembling ultra-thin dies. The 2007 edition placed a stronger focus on the formation of TSV.

It is interesting that the projection of chip thickness requirements on the 2005 and 2007 Roadmap editions, as well as on the 2008 update, were identical

Table 2.1 Minimum wafer thickness projections on ITRS 2005, 2007, and 2008 update

	2005	2006	2007	2008	2009	2010	2011	2012	2013
ITRS-2005	50[1]	25[1]	20[1]	20[1]	15[1]	15[1]	10[1]	10[1]	10[1]
ITRS-2007		50[1]	20[1]	15[2]	15[2]	10[2]	10[2]	10[2]	10[2]
ITRS-2008			20[2]	15[2]	15[2]	10[2]	10[2]	10[2]	10[2]

2014	2015	2016	2017	2018	2019	2020	2021	2022	2023
10[1]	8[2]	8[2]	8[2]	8[2]	8[2]	8[2]			
10[2]	8[3]	8[3]	8[3]	8[3]	8[3]	8[3]	8[3]	8[3]	
10[2]	8[3]	8[3]	8[3]	8[3]	8[3]	8[3]	8[3]	8[3]	8[3]

[1] Manufacturing solutions exist
[2] Manufacturing solutions are known
[3] Interim solutions are known
[4] Manufacturing solutions are NOT known

(Table 2.1). However, confidence in technology's capacity to provide manufacturing solutions sank after the first projections were made in 2005.

This change is an indication that the challenges in wafer thinning and thin die fabrication had been underestimated and, that today manufacturing solutions are known but not in place for manufacturing.

The need for ultra-thin chips today comes primarily from 3D system integration, where multiple active dies having active and lateral interconnects are vertically connected through TSVs. Such a 3D interconnect scheme allows for effectively shorter lengths of intermediate and global wires compared to the conventional planar IC.

As shown in Fig. 2.1, the effective interconnect length of the active wires will continue to increase strongly. This relates to the ever-growing complexity of interconnects. However, investment into more interconnect levels does not alleviate that problem (Fig. 2.1). The only remaining solution to overcome the interconnect bottleneck is thus to consider true 3D ICs, in which the interconnect routing can exploit both the lateral and the vertical dimensions [3]. As Fig. 2.1 shows this concept is clearly more effective than the conventional multilevel interconnects even, if only one metal level per stratum is provided. When one exploits both the maximum number of interconnect layers on chip and the maximum number of strata, the increase in active wire length over time becomes subtle. Certainly, this concept may not be feasible both from a technological and an economic point of view. The trend in wire length increase with technology advancement remains in spite of the best technological effort; this may relate to the fact that the projections

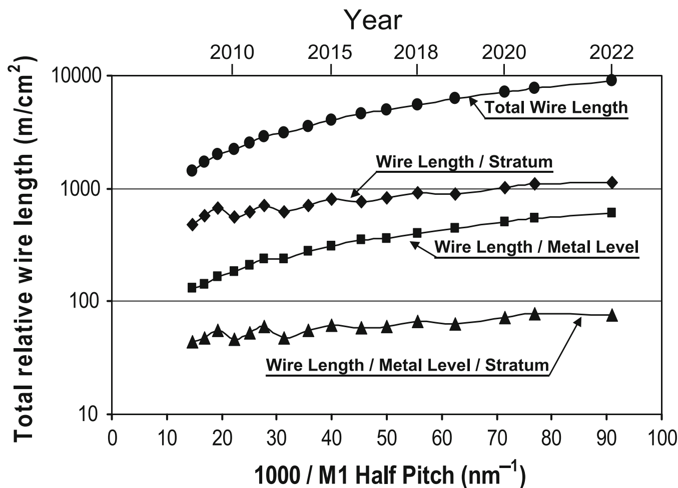

Fig. 2.1 Evolvement of the projection by the International Technology Roadmap for Semiconductors (*ITRS*) on total active wire length (M1 and intermediate interconnects) on chip. The wire length per metal layer, the wire length per stratum based on stratum dies having one metal layer only and the wire length per metal layer and stratum are calculated based on ITRS projections on the number of interconnect layers on chip and strata in 3D chips [2]

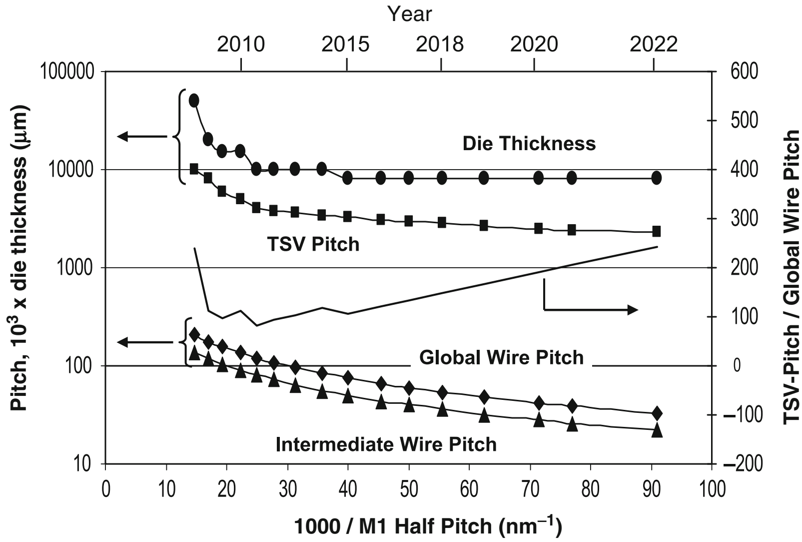

Fig. 2.2 Projection of the International Technology Roadmap for Semiconductors (*ITRS*) on global and intermediate on-chip pitch in comparison to the through-silicon via (*TSV*) pitch depending on die thickness. The calculated ratio of TSV and global wire pitch is large and will be increasing from 2010, thus indicating that utmost attention must be given to thin chip technology

on chip thickness assumptions, and thus on TSV pitch, have been too conservative. Figure 2.2 shows that from 2010 onward the advancement of global and intermediate on-chip interconnect pitch is stronger than that of TSV pitch. Unless the projections on chip thickness are revised in the coming editions of the ITRS, the effectiveness of TSV interconnects, indicated by the TSV/global wire pitch ratio in Fig. 2.2, will worsen over time. Note that the TSV pitch is directly related to the die thickness since, with current process solutions for via metal refill limit, the TSV depth/width ratio is 10:1 [2]. Clearly, considerably more attention must be put on ultra-thin chip fabrication techniques that can be made available for manufacturing [4].

2.3 Thin Chips for More than Moore

The 2005 edition of the ITRS first projected the need for focusing not only on device integration that relies on improvements in minimum feature size (More Moore) but also on applications leveraging silicon technology to provide added functionality (More than Moore). A need for thin chips was foreseen, e.g., in flip-chip packaging and chip assembly on flexible substrates and on textiles. Such applications rely less on electronic properties and technological advantages of

silicon than on its excellent mechanical properties, which have been known for a long time [5]. Silicon features high stiffness, quite comparable to that of stainless steel and cast iron and about three times the stiffness of aluminium (Table 2.2). Silicon is known to be brittle, but its ultimate strength is eight times that of stainless steel and 35 and 15 times better than the values for cast iron and aluminium, respectively. The overall better mechanical properties of silicon when compared to stainless steel and cast iron come with a more than double higher thermal conductivity, which is only somewhat lower than that of aluminium. Silicon is also considerably lighter than the other materials listed in Table 2.2.

Table 2.2 Properties of silicon in comparison selected metals

	Young's modulus (GPa)	Ultimate strength (MPa)	Thermal conductivity (W/mK)	Density (g/cm^3)
Silicon	185	7000	150	2.33
Stainless steel	200	860	43	8.19
Cast iron	210	200	80	7.87
Aluminum	70	480	235	2.70

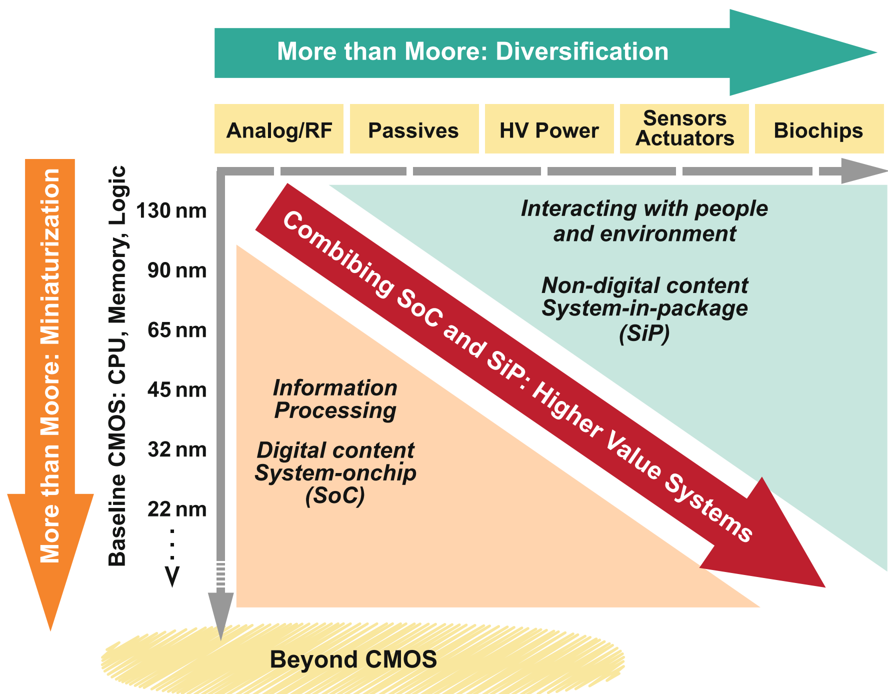

Fig. 2.3 Illustration of applications driven by strict miniaturisation according to Moore's law (More Moore), which may ultimately be superseded by novel device structures and physics (Beyond CMOS) and of applications of silicon technology providing added functionality and diversification (More than Moore)

References

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