

Contents

1	Introduction	1
1.1	Motivation	1
1.2	Original Contributions	2
1.3	Book Organization.	3
2	General Overview of Pipeline Analog-to-Digital Converters.	5
2.1	MDAC-Based Analog-to-Digital Converter Architectures	5
2.1.1	Two-Step Flash ADC	6
2.1.2	Pipeline ADC	7
2.1.3	Multi-Step Algorithmic ADC	8
2.1.4	Time-Interleaving ADCs	11
2.2	Building Blocks of Pipeline Analog-to-Digital Converters	12
2.2.1	Sample-and-Hold	13
2.2.2	Multiplying-DAC	14
2.2.3	Local Flash Quantizer and Comparators.	17
2.2.4	Operational Amplifier and Common-Mode Feedback Circuitry	18
2.2.5	Reference V/I and Buffering	23
2.2.6	Clock Generation	28
2.2.7	Digital Backend and Decimation.	29
2.3	Performance Metrics of Analog-to-Digital Converters	31
2.3.1	Static Performance Parameters	32
2.3.2	Dynamic Performance Parameters.	36
2.4	Overview and Comparison of Published Work	39
2.4.1	Two-Stage Opamps	39
2.4.2	Medium-Low Resolution High-Speed MDAC-Based ADCs	40
2.4.3	ADC Reference Voltage Circuitry.	42

3	Capacitor Mismatch-Insensitive Multiplying-DAC Topologies with Unity Feedback Factor	47
3.1	Conventional MDAC	47
3.1.1	Principle of Operation	47
3.1.2	Gain and Reference Shifting Error Analysis	48
3.1.3	Feedback Factor	50
3.1.4	Thermal Noise Analysis	50
3.2	Current-Mode Reference Shifting MDAC	52
3.2.1	Principle of Operation	52
3.2.2	Gain Error Analysis	54
3.2.3	Reference Shifting Error Analysis	59
3.2.4	Feedback Factor	63
3.2.5	Thermal Noise Analysis	64
3.3	Sampling Phase Reference Shifting MDAC	66
3.3.1	Principle of Operation	66
3.3.2	Gain Error Analysis	68
3.3.3	Reference Shifting Error Analysis	68
3.3.4	Feedback Factor	70
3.3.5	Thermal Noise Analysis	71
3.4	Performance Summary and Comparison of 1.5-bit MDACs	71
4	Application of Circuit Enhancement Techniques to ADC Building Blocks	73
4.1	Inverter-Based Self-Biased 1.5-bit Flash Quantizer	73
4.1.1	Principle of Operation	74
4.1.2	Circuit and Performance Analysis	77
4.1.3	Design Procedure	88
4.1.4	Performance Summary and Comparison	90
4.2	Two-Stage Inverter-Based Self-Biased Opamp	92
4.2.1	Principle of Operation	92
4.2.2	Circuit Analysis	95
4.2.3	Design Procedure and Optimization	112
5	Design of a 7-bit 1 GS/s CMOS Two-Way Interleaved Pipeline ADC	117
5.1	Specifications	117
5.2	Architecture	117
5.3	Implementation Details	119
5.3.1	Sample-and-Hold	119
5.3.2	CMRS Multiplying-DAC	121
5.3.3	Flash Quantizer	125
5.3.4	Opamp and CMFB	129

5.3.5	Switches and Clock-Bootstrapping Circuits	130
5.3.6	Clock Generator	132
5.3.7	Common-Mode Voltage Buffer.	134
5.3.8	Digital Backend	135
5.3.9	Decimator	137
5.3.10	Complete ADC.	139
6	Integrated Prototypes and Experimental Results	141
6.1	Two-Stage Inverter-Based Self-Biased Amplifier.	141
6.1.1	Floorplan and Layout	142
6.1.2	Design Considerations	143
6.1.3	PCB and Test Setup	144
6.1.4	Experimental Results.	146
6.2	7-bit 1 GS/s CMOS Two-Way Interleaved Pipeline ADC.	150
6.2.1	Floorplan and Layout	150
6.2.2	Layout Considerations	151
6.2.3	PCB and Test Setup	153
6.2.4	Employed Methodology for Tuning the Reference Currents	155
6.2.5	Experimental Results.	157
7	Conclusions	163
7.1	Final Remarks.	163
	Appendix: Solution for Current Reference Shifting Integration.	167
	References	171
	Index	181